DEVELOPMENT OF 3D RF MICROSYSTEMS USING ADDITIVE MANUFACTRUING TECHNOLOGY

A Dissertation
Presented to
The Academic Faculty

by

Fan Cai

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
May 2016

DEVELOPMENT OF 3D RF MICROSYSTEMS USING ADDITIVE MANUFACTRUING TECHNOLOGY

Approved by:

Dr. John Papolymerou, Advisor

School of Electrical and Computer Engineering

Georgia Institute of Technology

Dr. Christos Alexopoulos

School of Industrial & Systems Engineering

Georgia Institute of Technology

Dr. John Cressler

School of Electrical and Computer Engineering

Georgia Institute of Technology

Dr. Chuck Zhang

School of Industrial & Systems Engineering

Georgia Institute of Technology

Dr. Andrew Peterson

School of Electrical and Computer Engineering

Georgia Institute of Technology

Date Approved: [January 6th, 2016]

ACKNOWLEDGEMENTS

First and foremost, I would like to thank my Ph.D. advisor, Professor John Papapolymerou, for being the best supervisor that anyone could possibly ask for. His foresight in identifying problem as an important research area and his uniformly continuous support have made my professional graduate school experience rich and rewarding. I have always been amazed with the time and efforts that he spent on supervising students. More than the technical advice he gave, his generous mentorship beyond the academic has been and will continue to inspire me to strive for any success in my career. Moreover, his influence in my life makes it impossible for me to adequately express my respect and gratitude in words.

I also wish to express my deepest gratitude to Professor C. P. Wong serving as my co-advisor before he left for Hong Kong. Despite his busy schedule, he always made the time to give me invaluable advices on my research and life in a new country.

I would also like to thank my proposal and thesis committee members Professor John Cressler, Professor Andrew Peterson and Professor Chuck Zhang for providing helpful comments. I am especially indebted to Prof. Chuck Zhang for being my collaborators. Their active involvements and critical contributions are essential and irreplaceable for my Ph.D. project.

I am grateful to all members of Georgia Tech Microwave Circuit Technology (MiRCTECH) group. I am particularly indebted to Yuan Li, Arnaud Amadjikpe for their mentoring during the early part of my Ph.D. I wish to thank my colleagues, Spyridon Pavlidis, Outmane Chlieh, Christopher Barisich, Wasif Khan, Aida Vera, Carlos Morcillo, Gaetan Dufour, Sensen Li, for their support.

I also thank my friends such as Ziyin Lin, Wentian Gu, Nan Hua and others at GT for their valuable assistance during my time at Georgia Tech.

Finally but most important, I would like to thank my family for their love and patience, supporting me always when I needed it the most. They have always been infinitely kind, loving, and encouraging me to move forward.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS AND ABBREVIATIONS

λ_0	Signal propagation wavelength in vacuum in [m]
λ_g	Signal propagation wavelength in a wave-guiding structure in [m]
μ_0	Premeability of vacuum: 4π x 10-7 Hm-1
$tan\delta$	loss tangent of a dielectric substrate at a given frequency f
ε_{eff}	Effective permittivity of an electromagnetic-wave-guiding structure
c_0	Speed of light in vacuum: 2.99 x 108 ms-1
IL	Insersion loss in [dB]
RL	Returen loss in [dB]
NF	Noise figure in [dB]
TE	Transverse electric field/mode
TM	Transverse magnetic field/mode
TEM	Transverse electricomagnetic field/mode
3D	Three dimensional
GaAs	Gallium arsenide
LCP	Liquid crystal polymer (a kind of organic dielectric substrate)
CPW	Coplanar waveguide
CPWG	Ground coplanar waveguide
CBCPW	Conductor-backed coplanar waveguide
RF	Radio frequency

X band	8 GHz to 12 GHz
D band	110 GHz to 170 GHz
S parameter	Scattering paramter
SoC	System on chip
SoP	System on package
T/R	Transmit/receive
Rx	Receiver
TRL	Thru-reflect-line
SOLT	Short-open-load-through
LRRM	Thru-Reflect-Reflect-Match
NIST	National Institute of Standards and Technology
AJP	Aerosol Jet Printing
PP	Polyjet Printing
MLO	Multi-Layer Organic
AM	Additive Manufacturing
SL	Strereolithography

SUMMARY

In the last decade, there has been an increased interest in low-cost, low-power, high data rate wireless systems such as air defense systems, remote sensing radars and commercial applications like 4G communications. All of these applications require state-of-the-art fabrication technologies to push the limits on several design factors such as functionality, weight, size, conformity, and performance while remaining cost effective.

3-D printing technology as one of the potential alternatives of the photolithography or PCB, providing cost effective, fast production cycle, environmental friendly and complex components. Thus it is a good candidate for the fast prototyping integration of active circuits in 2-D and 3-D packaging configurations. In addition, many printable materials have not yet been explored for advanced package design that are thinner, lighter, and have better high frequency characteristics that make a wider range of applications possible.

This work intends to explore advanced 3-D integration for state-of-the-art components in wireless systems using various 3-D printing technologies. Several packaging techniques are discussed that utilize the inherent benefits of the 3-D printing techniques. The compatible materials of the 3-D printing system are assessed for their large processing format and compatibility with the build-up process. Single layer and multilayer interconnects, transmission lines are investigated at RF and millimeter-wave (mm-wave) to explore the benefits of each in terms of convenience, reliability, cost, and performance. For the first time，the operation frequency fabricated by 3-D printing is up to D band. A novel vertical via interconnect is applied to the integration of state-of-the-art system on package (SoP). Additionally, interconnects that route the signal directly from the chip interface to matching networks are implemented on novel flexible organic material PEN are designed.

This work also investigates the possible applications for cavity structures where the benefits of 3-D printing can be exploited for highly integrated receiver systems. Active and passive components are incorporated on LCP using a system-on-package approach to improve performance and enhance capability of the antenna. Wire bond interconnects are utilized as a convenient, low-cost packaging solution, ideal for prototype development.

CHAPTER 1

INTRODUCTION

Emerging applications in radio frequency (RF)/mm-wave regimes are placing a high premium on low-cost, compact and light-weight RF electronic components, while requiring multi-functionality at the same time. The development of RF front-end modules and their level of integration are continuous challenges in the aspect of fabrication techniques, and thus, there is a solid drive to employ an efficient fabrication method to meet the ever fast development of RF/mm-wave applications.

The boom in consumer popularity of portable wireless devices requires instant data, voice and video access and the escalation will go on as the big-data era has been approaching. Correspondingly, the demand for the wireless electronics industry with new and innovative technologies pushes the current state-of-the-art performance and functionality in a cost-effective manner. For example, the advent of smart phones, iPads, and tablet personal computers have been developed since 2001 because the third-generation (3G) mobile telecommunication networks gave birth to wireless internet access. New versions of products are released each year, integrating additional functionality with less space. Because of this, people's daily lives are altered in a fundamental way and trigger a series of technical companies. Nowadays, people are connected everywhere on-time. They not only enjoy video calling and media streaming but also share their on-time information and benefit from it. For example, people can take a ride from private drivers with lower price than a taxi or serve as a taxi driver during free time through Uber which is estimated as 50 billion dollars as a 4-years startup. This trend will progressively expand to finance, transportation, entertainment, service and machine monitoring. Who can deliver new ideas with a faster prototype and outpace other companies or researchers becomes an essential point in the fast-pace technology competition.

Figure 1. 3D printed structures.

According to this, the advent of 3-D printing technology offers a good option. Printed electronics employing solution-processed materials has received a great deal of attention in recent years and is able to realize low-cost large-area electronic systems. The versatility in printed RF circuit designs has been improving steadily with respect of printable materials, new functional RF components and new structures. On the other hand, the further improvement of the performance and the relationship with the characteristics of the printing technologies desired to be analyzed before 3-D printing can be adequate for a wide range of applications in terms of loss of signal lines, matching capability, noise figure for the front-end module, power handling of the filters and so on. This dissertation will investigate these issue from multiple perspectives and afford a practical way for 3D printing technologies on a wider RF applications.

1.1 3-D Printing Techniques

3-D printing technology has received growing recognition in recent years for possibly overcoming the limitations of the conventional 2-D planar fabrication methods,

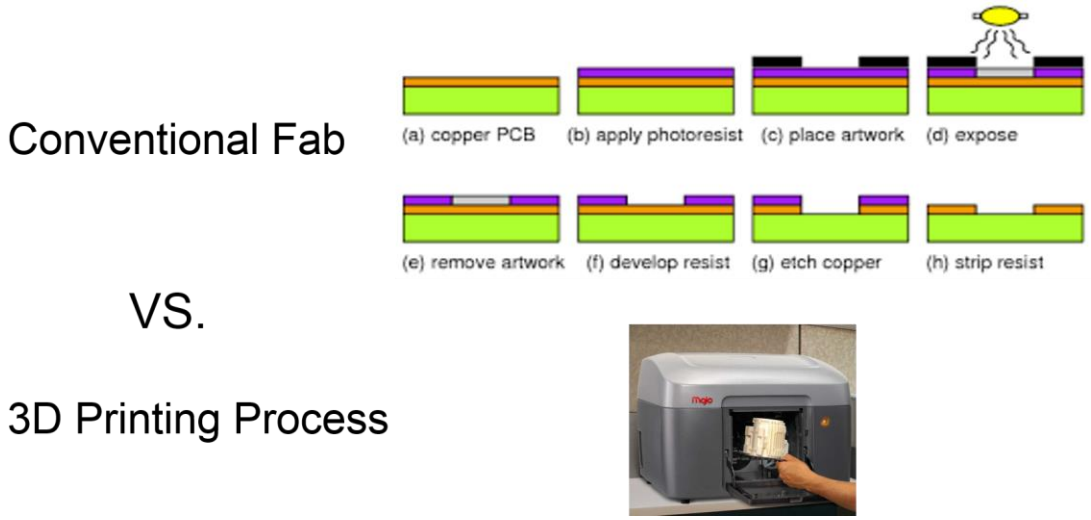


Figure 2. Conventional fabrication process steps versus 3D printing steps.

providing fast fabrication cycle, low-cost, environmental compliance, and mask free processing. Sometimes, it is also referred as an additive manufacturing method. They have been extensively utilized in many areas such as architecture, biology, medical, mechanics, and arts as shown in [1]-[5]. This advanced manufacturing technique has now been the next chapter in the industrial revolution from the early concept-to-proof investigation in academia. For instance, GE engineers produced model of a GEnx jet engine using an advanced 3-D printing technique called direct metal laser melting and the company has a plan to produce 100K additive parts by GE Aviation by 2020[6]. However, 3-D printing is still in the early stages of applications to the RF/mmW area.

Over the past decades, the subtractive methods, such as photolithography and PCB, have been the most dominant technologies for wireless circuit fabrication [7], [8]. A direct tradeoff lies between geometrical resolution and fabrication cost while maintaining a good performance. However, photolithography is a complex process including multiple steps such as etching, masking and electroplating (Figure 2). The high-quality maintenance of the facilities also brings a considerable amount of cost. In addition, some of the solvent and waste are corrosive and toxic to human beings. Meanwhile, PCB typically has limited resolution. In light of these issues, alternative fabrication techniques have been explored as

the key to realize low-cost large-area electronic systems for high performance and low-cost microwave circuits. The 3-D manufacturing technique shows the potential to provide a new paradigm for manufacturing low-cost microwave circuits.

First, 3D printing has few steps (1 or 2 step by printing) shown in Figure 2 which is the key feature taking along its other benefits. Owing to this intrinsic feature, it significantly reduces the fabrication cost and development cycle compared to the multiple-step sequence of photolithographic and chemical processing steps. Second, as a kind of additive manufacturing methods, it only deposits materials on the desired area and thus avoids extra waste. Last, the multidirectional ability of the process enables the printer to create a better overhang structure and frees RF circuit designs from traditional planar designs or limited multilayer designs. The various types of the 3D printers may also make new integration methods possible. All of the aforementioned advantages make the 3D printing technique as an economical and an environmentally friendly fabrication, specifically in the early prototype stage.

As most digital printing methods used in previous, inkjet-printed RF circuits have been demonstrated [9]-[14] for as RFID, antennas, inductors, MEMS and so on. Later on, other various 3-D printing techniques also emerged to be applied for RF applications. Although the performance of printed RF circuits and components have improved steadily with development of the treatment on the substrate, printable materials and hybrid printed methods, their performance generally is inferior to that of traditional fabrication methods and restricted for many substrates. Therefore, printed electronics need to overcome a barrier in order to be productively applied to the commercialization of printable RF microsystems. In this dissertation, the most advanced digital printing techniques will be discussed and selected properly for specific RF applications and show state-of-the-art RF performance by 3-D printers.

1.2 Printed Interconnects

While the current licensed band has become more crowed and insufficient for the growing demand, high-band has been extensively explored over the past decades. Recently, silicon transceivers operating in the D-band (110-170 GHz) have grown steadily because the D-band is a good candidate for tremendously fast communication applications such as 10-50 Gb/s wireless I/Os for chip to chip communications and high resolution imaging technology. Over the past a few years, mm-wave has been validated with the corresponding chips [15]. Accordingly, packaging technologies, such as system-on-chip (SoC), system-in-package (SiP), and system-on-package (SoP), have been investigated to integrate an increasing number of functional components with a reduced size. Compared with SoC, SoP has more design flexibility to achieve the whole system performance optimization by its inherent capability of integrating heterogeneous MMICs based on different technologies such as Si, SiGe and GaAs [16]. The liquid crystal polymer (LCP) multilayer technology to integrate passives and actives at the packaging level has been developed [17], [18]. The multi tiers of layers stacked upon each other in the third dimension can reduce the communication latency among various functional tiers.

Transmission lines and passive circuit elements occupy over 50% percent areas of the whole board and account for a large percentage of the cost. To a large extent, the restriction in the implementation of high-speed transmission lines, interconnections and passive circuits impede the development of both the reduced size of the system and additional functionality.

So far, the reported work limited the wider application of digital printing technology for RF/mm-wave applications as there is a lack of study on the effect of these passives and interconnects for the further integration of a system. Shaker et al. [19] reported inkjet-printed 90 Ohm CPW lines with a loss of 2.8 dB/mm at 100 GHz that is not acceptable for practical usage and Oscar et al. [29] presented the inkjet-printed CPW lines up to 25 GHz and showed a loss of 0.27dB/mm at 20 GHz. The resolution of inkjet printing

was around 100 μm. At low frequencies, the effect of the conductor loss due to the metal resistivity and surface roughness is usually acceptable. However, at higher frequencies, the surface roughness becomes comparable with the skin depth of the metal, thus making a much more significant impact on the passive loss. What's more, the reduced wavelength at higher frequency makes it sensitive to the geometrical fabrication tolerance which determines the impedance matching.

To further demonstrate multilayer stacking capability by 3-D printing, [30] presented a multilayer patch antenna with an additional dielectric layer deposited between the host substrate and the conductive silver ink layer on the top. However, inkjet printing is unable to fabricate sharply curved edges and small gaps less than 100 μm, limiting its applications in a more complicated structure. In addition, for multilayer RF structures, alignment function and vias are highly critical. So far, alignment function has not been integrated with an inkjet printer. For example, [30] claimed a 130 μm misalignment for a 3 μm thick silver ink layer. Later, a 75-μm diameter via with 0.1 Ω resistance and a 400 μm diameter via with 0.05 Ω are demonstrated in [13] through 700 nm PVP films. However, the aspect height ratio was limited and the vias were printed twice with the substrate which gave challenges for the fabrication. Besides, inkjet printing applications are still restricted below 20 GHz due to the limited resolution of 50–100 μm. What's more, the intrinsic mechanism of the machine causes a frequency clogging problem and thus inhibits the mass production.

As another type of additive digital process for printed electronics, Aerosol Jet Printing (AJP) technology is able to address the aforementioned fabrication issues. It is a more advanced technique compared with inkjet printing since its feature size can go down as small as 10 μm. Note that the resolution of inkjet printing is typically 50–100 μm as mentioned above, which is 5–10 times larger than that of AJP. What's more, there are more material options for AJP than inkjet printing, including conductive, semi-conductive,

resistive and isolating materials. The AJP system also improves the alignment function, non-planar printing capability and continuous stream of printed ink. In all, AJP can solve the common restrictions of most digital printing technologies while keeping the benefits of a digital approach such as time efficiency, less waste and less cost. So far, no literature has reported AJP at the millimeter-wave frequency range. This dissertation will investigate AJP for building wideband interconnects from DC to D band as well as its applications for multilayers stacking and transitions with embedded vias.

1.3 Printed Cavity Resonators/Filters

The third objective of the dissertation is to investigate cavity structures by 3-D digital printing. Resonators/filters are widely used as key functional devices in communication systems for RF applications. A filter is a linear circuit whose primary purpose is to pass desired frequencies while rejecting others. Planar technologies are put aside because their limited quality factor or unloaded Q_u (less than 200) will inevitably harm the in-band insertion loss. On-package integrated cavity filters fabricated by digital printing is a very attractive option for 3-D RF front-end modules because of their relatively high quality factor (Q) and low loss compared to planar filters

To date, the well-proven techniques to build cavity filters include low temperature Co-Fired Ceramic (LTCC) and Multi-Layer Organic (MLO) techniques which have been the dominant methods for 3-D system on package (SoP) RF front ends [7], [8]. These techniques are not only costly, but also show relatively increased complexity. The conventional microwave resonators and waveguides made of metal are heavy and bulky while costly to manufacture.

In contrast, the digital printing technique offers a much simpler way to build a complex 3-D structure without the burden of achieving high aspect height ratio while getting rid of time consuming steps, being highly repeatable, and largely reducing the new

prototype manufacturing cost. 3-D printing technology for RF structures was primarily implemented by strereolithography (SL) due to its fine feature size of 50 μm. Most recently in [19], it has been demonstrated that a horn antenna was printed by Fused Deposition Modeling (FDM) with ABS plastic and coated by conductive spray. This process is low-cost whereas the resolution is above 100 μm. Furthermore, the surface roughness is around 60 μm which is prohibitive for RF applications where the quality factor is a major concern.

1.4 Heterogeneous Integration by Printed Substrate On-Demand

With the proposed fabrication of passives by 3-D printing technologies, it is worthy of also demonstrating the feasibility of using 3-D printing technologies for wireless application with integrated active devices. In the current cost-competitive wireless market, a low-cost package and fabrication technology is preferred. These challenges motivate the designers to look beyond just the electrical performance of individual components to a system-level module integration approach. The ever increasing demand of operating speed to meet the big-data era put the new challenge for the well-established infrastructure. Thus, it is valuable to investigate the potential utilization and the limitation of the possible package schemes for wideband applications.

This dissertation demonstrates a tailorable substrate on demand by 3-D printing and implements a broadband superhetrodyne receiver based on tailorable substrate. The method uses Polyjet Printing technology, which is a branch of emerging additive manufacturing technologies, to tailor the substrate with designed cavities for thin film dies. This results in reduced parasitics and loss to the package, thus not affecting the die's original performance without the compromise of additional design steps. It shows the flexibility of exploiting a new interconnect methodology integrating heterogeneous semiconductor technologies.

In this dissertation, the most advanced 3-D printing technologies will be assessed for RF applications. This dissertation will be outlined as follow: Chapter 2 reviews multiple popular 3-D printing techniques and assesses the printing features of the advanced fabrication techniques (AJP and Polyjet Printing) used to build structures in this dissertation. Chapter 3 investigates the single layer high-speed interconnects and active circuit designs based on 3-D printing. Chapter 4 extends the single layer interconnects to multilayer interconnects as well as the wideband multilayer transitions. Chapter 5 develops cavity resonators and filters and proposes a practical solution to take into account the surface roughness effect which is a noticeable and serious problem limiting RF performance. Chapter 6 presents the characterization of printable materials and a broadband integration of heterogeneous MMICs by 3-D printing.

CHAPTER 2

PRINTING TECHNOLOGIES

This dissertation explores adequate fabrication processes among advanced additive manufacturing methods to offer a robust, economical, time-efficient and environmental-friendly way that allows for RF/mm-wave applications.

These additive processes are the inverse of traditional manufacturing methods that typically mill away or subtract the surfaces until a product is finished. The traditional desired fabrication method using photolithography process is an expensive and complex one. The high-quality maintenance of the facilities brings a considerable amount of cost and it is disturbing to have a wide usage of corrosive and toxic solvents during photolithography [21]. On the other hand, though PCB is a low-price option for budget consideration, typically it has limited resolution [22]. The 3-D manufacturing technique affords a new paradigm for manufacturing low-cost microwave circuits.

Additive manufacturing (AM), or 3-D printing as it's better known, refers to various processes used to synthesize 3-D objects purely controlled by a computer via a CAD software. The unique characteristic of 3-D printing lies in the fact that it has the capability of directly depositing materials without any predefined master pattern on desired areas with little waste. Namely, it can deposit ink to any arbitrary positions on a substrate by means of precisely controlled movable nozzles and a plate on which substrates are loaded.

Recently, versatile RF circuits by 3-D printing have been demonstrated as RFID, waveguides, sensors and antennas [24]-[27] due to their inherent low cost and compatibility with low-cost substrates. However, their performance generally is inferior to that of conventional counterparts and not enough analysis is given to clearly explain that. In [24],

Chieh *et al*. report a Ku-band corrugated horn antenna using 3-D print technology with a gain of 19 dBi but conclude that the loss is either due to the conductivity of the metal spray or the plastic underlay , thus, it is unknown the main source of the loss. Cook *et. al.* describe a wideband antenna on paper substrate from 2-10 GHz and simply assume the loss is from the substrate. Shaker *et al*. [19] report inkjet-printed 90 Ohm CPW lines with a loss of 2.8 dB/mm at 100 GHz that is not acceptable for practical usage but didn't indicate the reason of additional loss. These inexplicit results of individual components stand in the way of further integration of RF system. Thus it is necessary to provide a relationship between the printing technologies and the RF performance.

This chapter describes the fabrication process, the technology assessment to provide necessary information for the RF/mm-wave applications in the following chapters. In 2.1, AJP is proven to have the finest resolution among all of the digital printing technologies, was realized successfully and multiple materials by the printer were achieved. The conductivity of the sintered silver structures was half of that of bulk silver after sintering at temperatures up to 200 ^{o}C. In 2.2, Polyjet Printing technology is reviewed and compared with other advanced technologies.

2.1 Features of 3-D Printing Technologies

2.1.1 Cost

The market penetration rate of 3-D printing technology into the highly competitive wireless consumer electronics market largely depends on the cost. The costs stem from materials, reduced tooling and assembly costs as well as the initial investment in machine. A study from McKinsey & Company [20] shows that the machines and their maintenance typically account for 40 to 60 percent of total printing costs. The materials used in the manufacturing process can account for 20 to 30 percent when using common materials

Table 1 Comparison of cost by photolithography (conventional manufacturing process), AJP, and PP (3-D printing methods).

	Photolithography	AJP	PP
Initial Investment (M dollars)	1000	~0.3	~0.3
Cost/inch with 1 inch^2	200-500 $	1-5 $	2-3 $
Cost/inch with 10 inch^2	50-100 $	1-5 $	2-3 $
Cost/inch with 100 inch^2	5-10$	1-5 $	2-3$

such as aluminum, or 50 to 80 percent when printing with exotic materials such as titanium. Labor and energy make up the rest. In traditional manufacturing process, the complexity

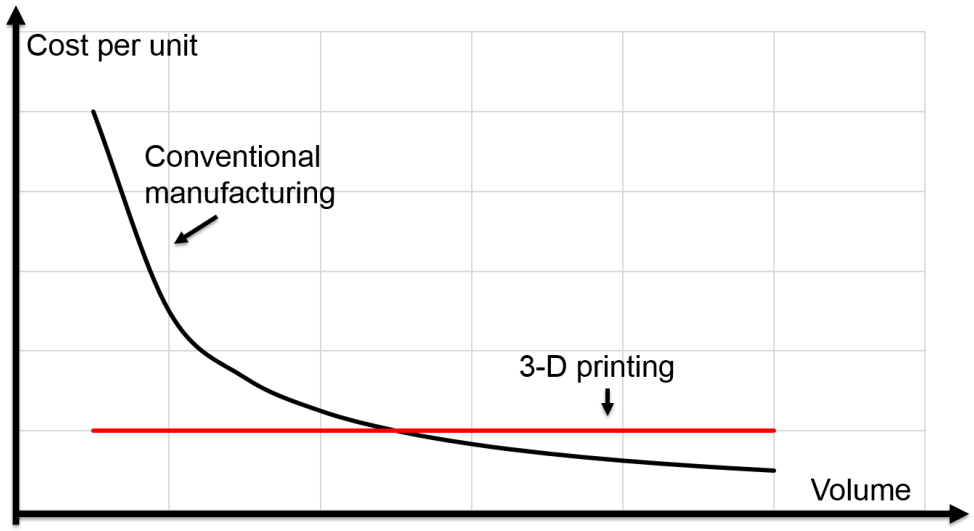


Figure 3. Comparison of cost per unit by conventional manufacturing processes and 3-D printing methods.

increases costs, so there should be a tradeoff between the complexity and cost for the total market. If the 3-D printing has a comparable performance as traditional manufacturing processes, however, it does not face these structure barriers. Considering the initial investment, cleanroom facilities are generally over 1 billion dollars while the advanced 3-D printers are ranging from 100 k-500 k dollars. Without taking this into consideration, the

initial cost for each unit of output is pretty high for prototypes and decreases as volumes increase by conventional fabrication process because of masks or molds is required. It is also restricted from variation of designs. Oppositely, the cost is relatively constant by 3-D printing process and independent of the volume or variation of the designs. The comparison of cost are plotted in Figure 3.

Take photolithography fabrication process as an example, it costs over 200 dollars to fabricate 1 inch copper pattern on commercial substrate for the most simple one layer substrate and reduces to less than 10 dollars when the pattern is over 100 inch. If use Aerosol Jet Printing (AJP) and Polyjet Pringing (PP) as representatives for advanced 3-D printing methods, they cost less than 5 dollars using silver ink and this cost are constant as the product volume increases. An approximate cost analysis is listed in Table 1.

2.1.2 Time

Besides 3-D printing's capability to increase geometric complexity, it is superior to conventional manufacturing methods as a fast prototyping method, with regard to time. Even with a distinction of a higher degree of integration in circuit designs, 3-D printing does not add trivial work which arises during lead times, process time and managing inventories. Rate of yielding product is neither effected by multilayer stacking for individual material. The relationship between the complexity of structures and the product volume is shown in Figure 4. There is a tradeoff between the printing resolution and printing speed. Generally, the faster the printing speed, the lower printing resolution.

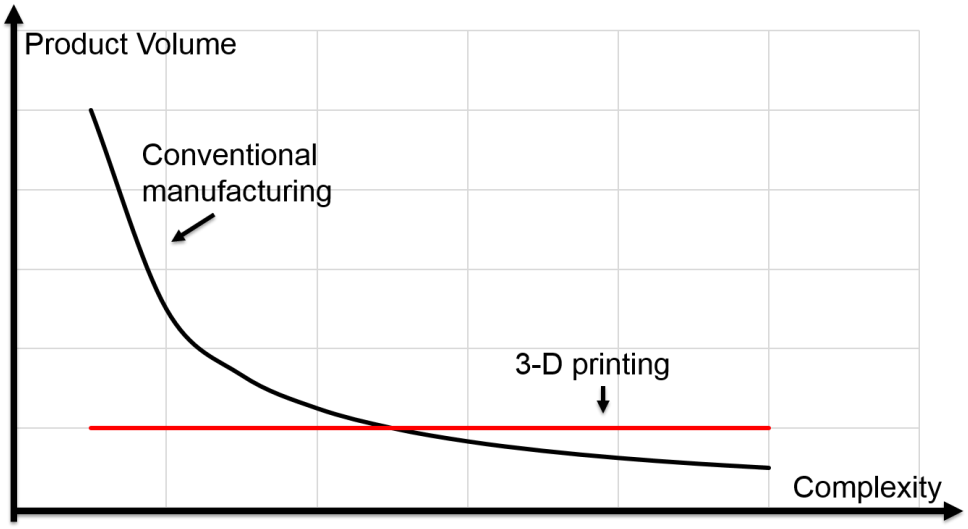


Figure 4. The relationship between the complexity of structures and throughout of products.

However, the printing speed is also related to technology. Both time and cost are mainly depend on the total volume of materials consumed.

2.2 Aerosol Jet Printing (AJP)

2.1.1 Basic Principle of AJP

Aerosol jet printing is an additive digital process for fabricating printed electronics, structural and biological patterns with fine-feature size. The whole process operates under atmospheric conditions and eliminates the requirement for clean room environments, such as those used for traditional photolithography processes. It could solve the common restrictions of the most digital printing technologies while keeping the benefits as a digital approach. For instance, AJP process is capable of controlling pattern deposition with higher resolution compared with inkjet printing, and thus is appropriate for millimeter wave circuit designs. Due to its wide materials options and high resolution, an AJP systems is able to

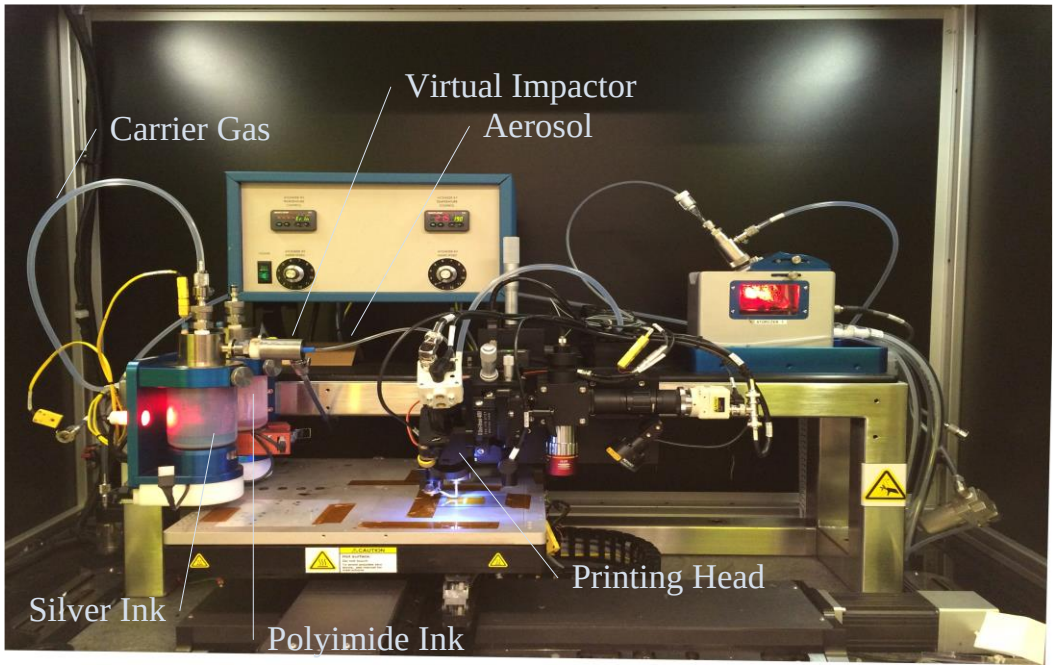


Figure 5. AJP system at Georigia Institute of Technolgoy.

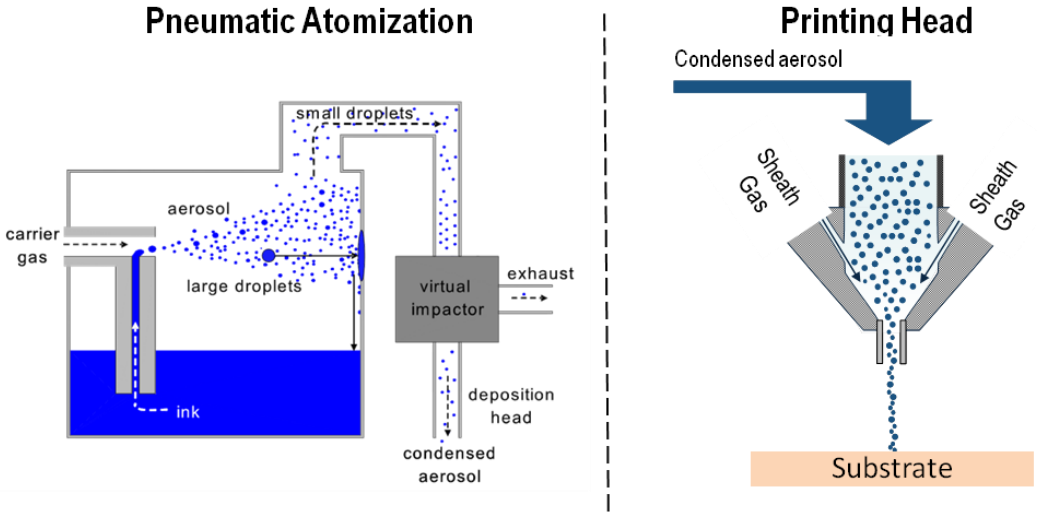


Figure 6. Principle of pneumatic atomization.

deposit metal and dielectric materials as well as other new materials, such as nanotubes and grapheme.

An AJP printing system is shown in Figure 5. The machine is able to print multiple materials at the same time. The deposition process begins with atomizing liquid ink into an aerosol, with a droplet size from 1 to 5 μm. The atomization process can be done by using either a pneumatic or an ultrasonic atomizer. In this dissertation, all the samples were fabricated with pneumatic atomization. The output stream goes through the virtual impactor where the stream is further refined. Then the aerosol stream is directed to a print head and aerodynamically focused by a coaxial sheath gas flow. The sheath gas stream prevents contact between the aerosol stream and the inner cladding of the print head nozzle.

Due to this novel fundamental principle, the AJP technology delivers the finest resolution among digital fabrication methods with a much lower probability of clogging issues because of the non-contact droplets. Table 2 lists the current printing technologies and compares their performance. There are three main printing technologies based on droplet, flow and tip. The operation principle of the AJP is similar to inkjet printing with regard to the printing mechanisms. However, AJP overwhelms inkjet printing in terms of the resolution and the capability of forming complex curvature patterns. AFM provides the finest resolution but it shows a substantially slow writing speed that is not practical for printing RF/mm-wave circuits.

Table 2 Comparison of different direct write processes

DW processes		Resolution	Write Speed	Complex curvature printing
Droplet	Inkjet	50-200 μm	0.3 mm/s	Moderate
	Aerosol jet	10-150 μm	0.25 mm/s	Excellent
Flow	Micropen	100 μm	50 mm/s	Excellent
Tip	AFM	12 nm	0.2-5 μm/s	Limited

Moreover, for AJP, it has wide material options that bring the technology to broader applications. Materials with a viscosity range from 1 to 1000 cP are compatible with the printing system. Some printable materials have been tested including but not limited to: metal nanoparticles, carbon nanotubes, graphite, silver ink, polyimide and so on. Meanwhile, the substrates could be either flat organic materials/metal or a 3D surface.

2.1.2 Materials Characterization

Silver ink and polyimide are used as conductive traces and the dielectric substrate to build RF and mm-wave circuits in this work. Therefore, the RF properties of these materials including the dielectric constant and loss are fully characterized. The characterization details are discussed in the following section.

A. Silver Ink

A silver nano-particle suspension in hydrocarbon solvent was purchased from UT Dots. The silver ink contained 30-50 wt % of silver nanoparticles with the particle size ranging from 7- 10 nm. The viscosity of the ink was between 35-45 cP. Figure 7 illustrates the characterized minimum feature size of the silver ink on substrates. For a single layer, 10 μm gaps and 10 μm line-widths, with less than 1 μm deviation, were repeatedly achieved. The nozzle size could be changed from 100 μm to 300 μm in order to get the

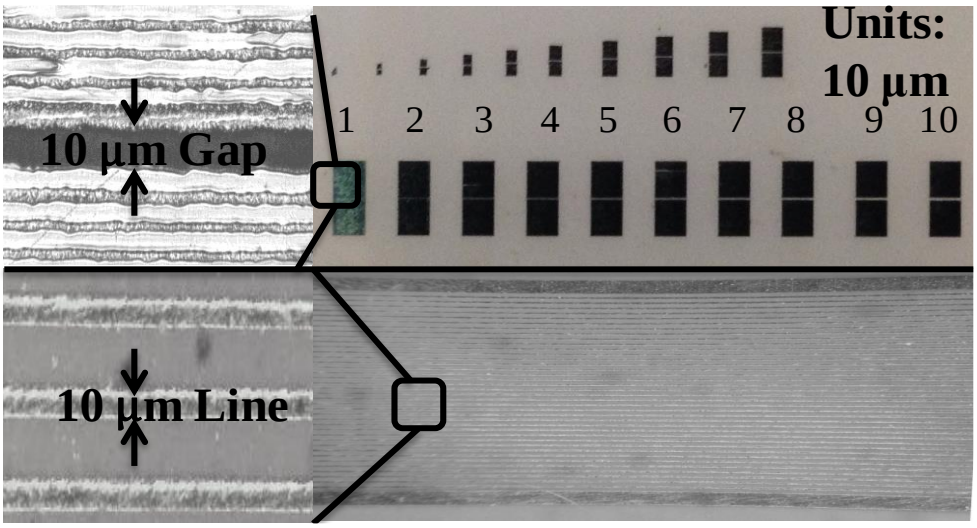


Figure 7. Printed lines and gaps with silver ink.

minimum resolution from 10 µm to 100 µm. Therefore, it can fill a specific printing pattern with an optimized resolution and fabrication time. The speed of the printing stage was maintained at 3 mm/s. The fabrication was conducted with an atomizer gas and sheath gas flow rate of 700 Standard Cubic Centimeters per Minute (SCCM), and 47 SCCM, respectively. The printing stage was kept at 20 °C during the entire printing process.

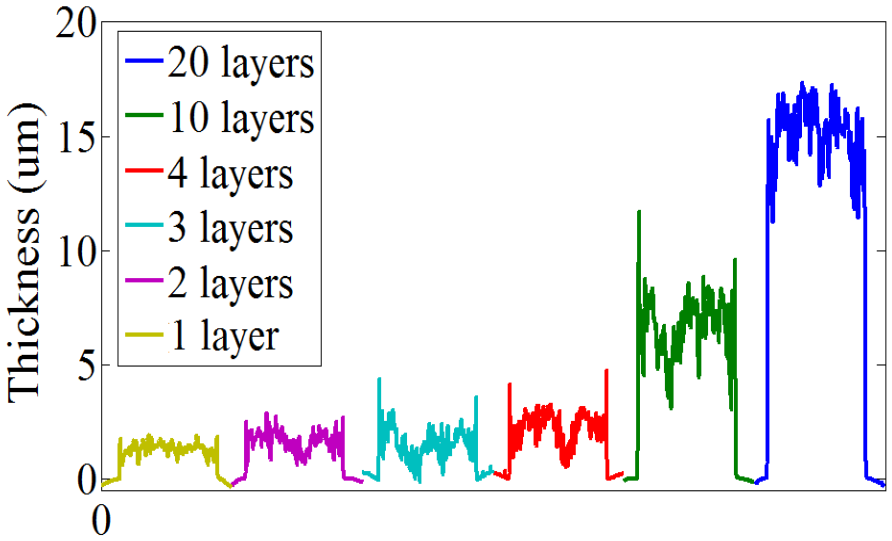
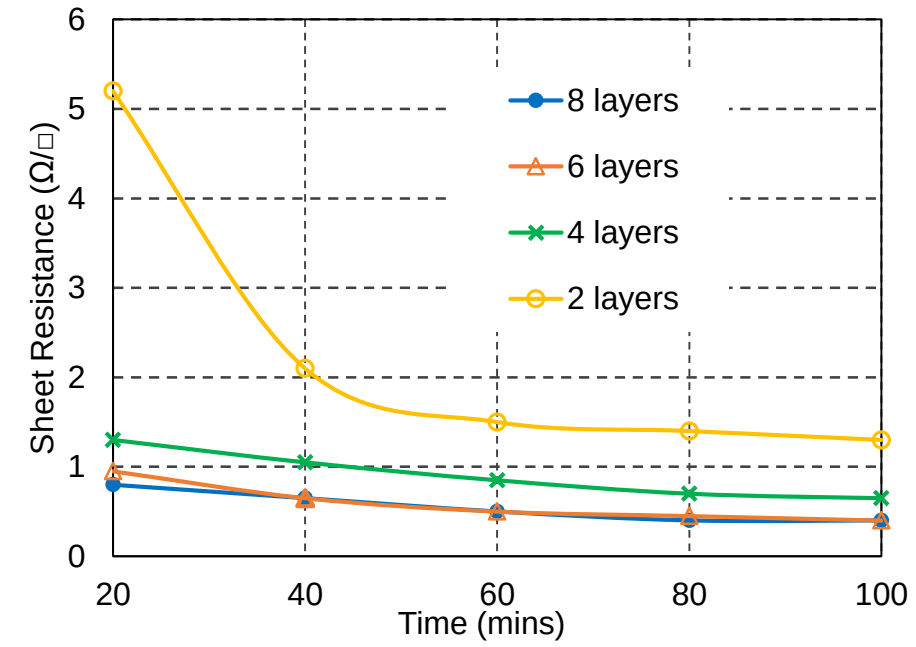


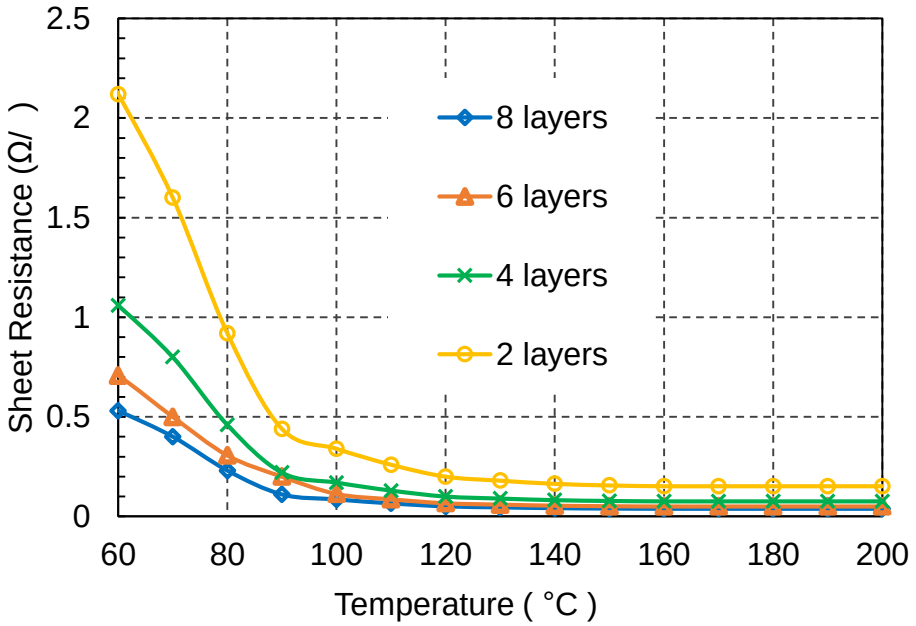
Figure 8. Measured thickness of the silver ink vs. numbers of the deposited layers.

The thickness of the printed metal layers up to 10 layers was measured using the Dektak profile meter. The measured data in Figure 8 shows that it was approximately 0.7 μm/layer and the surface roughness increased along with the number of stacked layers. The averaged surface roughness was around 2 μm with 7 μm thick silver ink.

To figure out the performance of the radiation loss and ohmic loss, we need to know the conductivity and the thickness of the metal layers. The conductivity of the silver ink was affected by the curing temperature after a deposition. It was calculated by sheet resistance. Figure 9 shows the sheet resistance versus numbers of printed layers at different sintering temperatures. The sheet resistance was measured using a 4-probe testing module with a Keithley 2400 source meter. The sheet resistance decreased drastically with increasing sintering temperatures and number of the printed layers below 200 °C, and then decreased slowly over 200 °C. After curing with a certain time (~ 1 hour), the sheet resistance of the silver ink become stable.



(a)



(b)

Figure 9. (a) The sheet resistance of the silver ink with various number of layers versus the curing time at a temperature of 150 ℃. (b) The sheet resistance of the silver ink with various number of layers versus the curing temperature after 60 mins of curing.

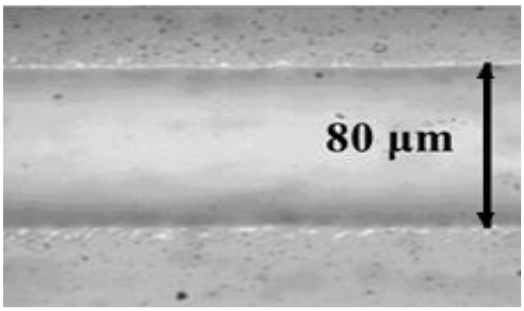
B. Polyimide

As a proof of the concept, polyimide was chosen as the dielectric material for our RF designs due to its wide applications in commercial products and stable performance. Other compatible materials, such as SU-8, graphene, CNT can also be used if their viscosity are within the range.

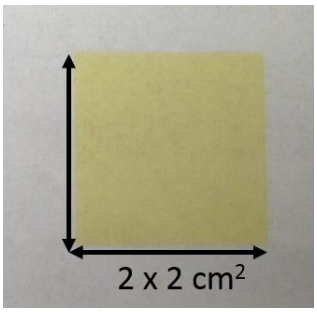
The viscosity of the polyimide ink was 500 cp. The fabrication was conducted with atomizer gas and sheath gas flow rates of 600 Standard Cubic Centimeters per Minute (SCCM) and 60 SCCM, respectively. Exhausted gas flow rate was controlled at 577 SCCM. A 300 μm nozzle was used for large area polyimide printing. The width of a single polyimide line is 80 μm shown in Figure 10 (a). It is evident in this figure that the resulting printed polyimide had superior edge and surface roughness than the silver ink, with an edge error of 2%. While a comparably large nozzle is used, the process is adequate to form a larger pattern shown in Figure 11 (b). A 2×2 cm^2 pattern takes only 5 mins, meaning that AJP is able to form the entire substrate in a front-end module with a very fast printing time.

The thickness of the printed polyimide by profilometer is shown in Figure 12. The thickness of each layer was 0.65 μm ± 0.05 μm. When printing a polyimide layer with a thickness less than 5 μm, the surface roughness was less than 0.5 μm; while the surface roughness was approximately 2 μm for 60 μm-thick polyimide. However, Figure 12 shows that the linear relationship between the thickness of the polyimide and the corresponding number of layers cannot be kept beyond 30 layers. Therefore, a fully curing process is required with each 20 μm polyimide (30 layers). What's more, the surface quality also degrades along with the increasing number of layers as seen in Figure 8 and Figure 12. The edges of the pattern are much higher than the center while the edges are almost flat when the thickness is less than 5 μm. This is because the tensile force at the edge is negligible when the total thickness is small, but it starts to take place when the number of layers increases. The initial experiments indicate that in order to achieve a uniform quality of

polyimide and prevent the internal solvent from escaping, each batch of the deposited polyimide layer should be less than 20 μm.



(a)



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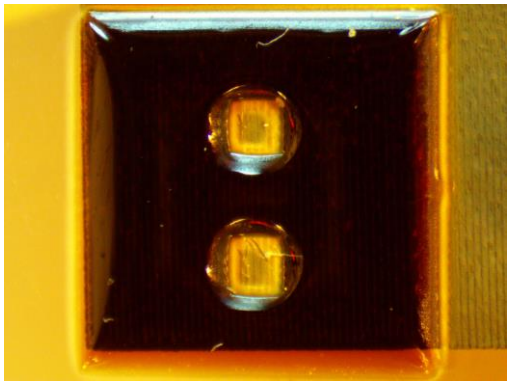


(c)

Figure 10. Printed structures based on polyimide: (a) a single line with a width of 80 μm; (b) a printed rectangular pattern of 2cm×2cm; (c) printed vias with a diameter of 400 μm and a height of 100 μm.

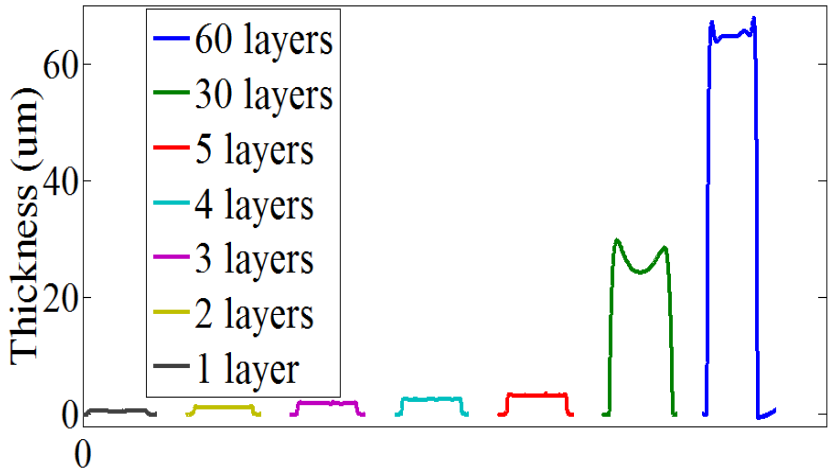


Figure 11. Prolifometer measurement of the thickness of the polyimide.

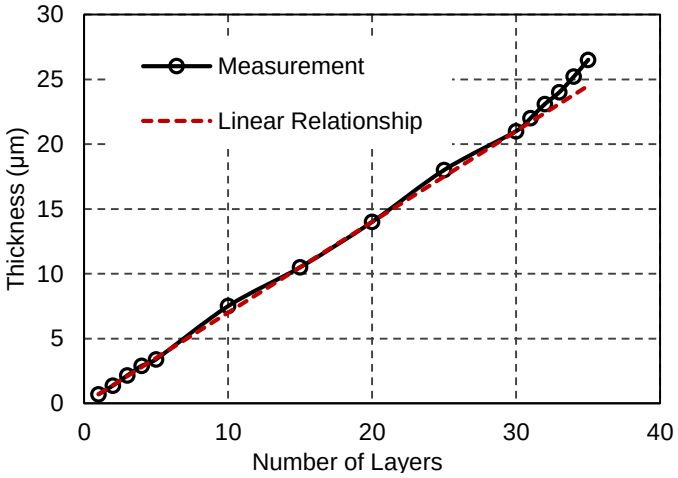


Figure 12. The relationship between the thickness of the polyimide and the corresponding number of layers.

2.3 Polyjet Printing Technology

Among 3-D printing technology, there is another type of additive manufacturing technique that aims to build 3-D structures with cavities. These 3-D printing technologies can automatically build the model from the 3-D drawings in the computers. In contrast, both inkjet printing and AJP are based on 2-D patterns and then stack multilayer 2-D

patterns to form the final 3-D structures. Fused Deposition Modeling (FDM) and Polyjet technology are the two of the most advanced technologies.

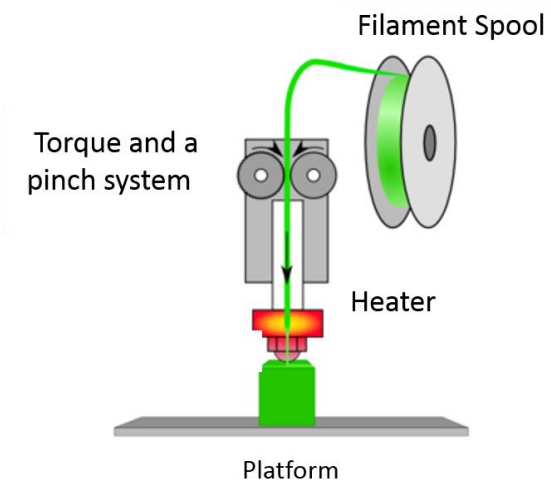


Figure 13. Operating mechanism of the FDM [40].

FDM is by far the most popular 3-D printing technology. This technique creates rigid and functional parts based on generating the filament of a materials (such as plastic or metal). Software slices and positions a 3-D CAD file and calculates a path to extrude thermoplastic. After that, the printer builds the model, and the operate process is shown in Figure 13. First, the filament goes through the torque and a pinch system to the heater where it is melt, then it is forced out at a smaller diameter and laid down on the model where it is needed. By adjusting the material feed rate and print speed, the thickness can be controlled while also eliminating space between lines. The supporting material is able to be dissolved in detergent and water or breaks away manually.

This technology generates unrivaled performance in mechanical, thermal and chemical strength because of the high-performance thermoplastics that can be built as end-use parts in standard. For example, these materials include Acrylonitrile butadiene styrene (ABS), Polycarbonate (PC), Polyethylene terephthalate (PET) as well as other commercial materials. More materials are continuously developed. While FDM is able to create rigid

parts, it is not suitable for flexible parts due to the limit of materials options. The surface finish is 50-100 μm.

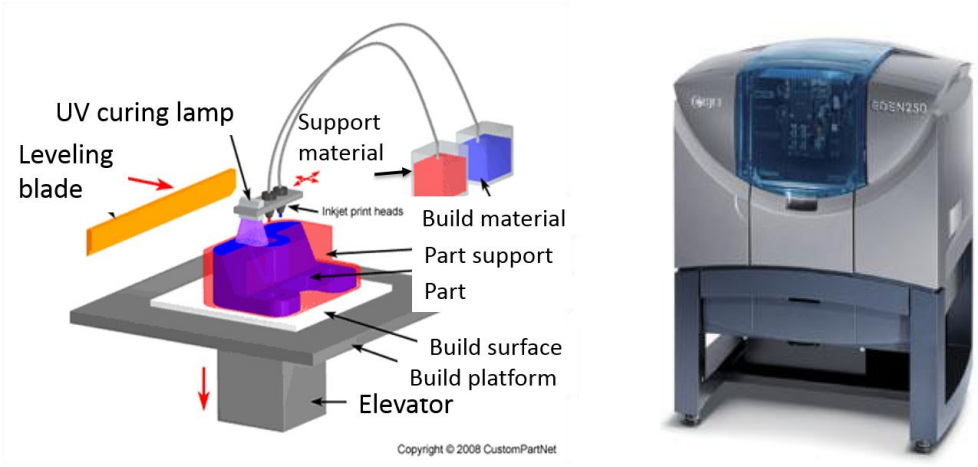


Figure 14. Operate mechanism of the 3-D Polyjet Printing system [42].

Table 3 Performance comparison

	FDM	Polyjet Printing
Process Time	Moderate	Fast
Surface Finish	Bad	Excellent
Feature Detail	Bad	Excellent
Flexible	Bad	Excellent
Durable	Excellent	Moderate
High-performance	Excellent	Bad

3-D Polyjet Printing technology, which is the most detailed and precise printing method, is based on a distinctively different printing mechanism shown in Figure 14. It jets

layers of liquid photopolymer onto a build tray and instantly cures them with UV light. The Eden 250 system pictured in Figure 14 (b) is the 3-D Polyjet Printing machine used at Georgia Institute of Technology invention center. The material used in the system is UV curable resin. 3-D Polyjet Printing is capable of high-quality rapid prototyping with the highest accuracy among all the 3-D printers. The superior surface finish, fine details, and durability make this technique suitable for RF applications. The system contains 3-D printer jets and instantly UV-cures tiny droplets of liquid photopolymer. The same as FDM, the complex and overhang shapes are formed by the removable gel-like support material, which can be easily removed by hand, or with water. The final performance of the parts will be determined by manufacturing tolerances and the surface roughness. Polyjet is able to provide parts with a near-paint-ready surface. The surface roughness was found to be approximately 0.5 μm when the surface plane is parallel to the printing direction. However, this could be significantly distorted when this is perpendicular to the surface plane, or sacrificial materials exist. The lateral resolution of Eden is >15 μm, while the vertical resolution is 16 μm.

The general performance of FDM and Polyjet Printing (PP) are compared and listed in Table 3. While each application shares requirements as well as distinct demands, it is application-specific demands that ultimately decide which is the best tool. For example, in our application, when the frequency goes higher than 10 GHz, the skin depth of copper is around 1 μm, so that FDM with a surface roughness around 50-80 μm will significantly degrade the RF performance. In this case, the high resolution and fine feature details as hallmarks of the Polyjet process will benefit more for RF/mm-wave applications.

In this dissertation, the Polyjet Printing is applied for microwave components for the first time which features the highest profile-accuracy (16 μm per layer), excellent surface finish (less than 1 μm) and low production cost compared with photolithography. In [5], extensive studies have been performed to show that the fabrication error of the PP

is only 2.14%, providing great potential for RF/millimeter-wave cavity waveguides. Compared with photolithography, the PP fabrication process is much faster and cleaner. Moreover, it does not require post curing for materials, and thus, it is superior to the polymer based 3-D printing technique.

CHAPTER 3

D-BAND BROADBAND TRANSITIONS BY AJP

3.1 Background of D-band Interconnects

The current licensed band has become more crowed and insufficient for the growing demand and, thus, a high-band has been extensively explored over the past decades. Recently, silicon transceivers operating in the D-band (110-170 GHz) have grown steadily because D-band is a good candidate for tremendously fast communication applications such as 10-50 Gb/s wireless I/Os for chip to chip communications and high resolution imaging. Over the past a few years, mm-wave has been validated with the corresponding chips [15]. The recent technology like inkjet printing technology is not suitable for such a high frequency application (wavelength is approximate 1 mm) due to the limited resolution.

Shaker et al. [19] reported the inkjet-printed 90 Ohm CPW lines with a loss of 2.8 dB/mm at 100 GHz that is not acceptable for practical usage and Oscar [29] presented the inkjet-printed CPW lines up to 25 GHz and showed a loss of 0.27dB/mm at 20 GHz. The resolution of inkjet printing is 50-100 μm, depending on the size of nozzles. Recently, extensive efforts have been made to improve the resolution by two ways: reducing the size of the nozzles which has been down to 20 μm; making surface treatment to form narrower lines. While the size of nozzles faces bottleneck to be further reduced, the smaller nozzles increases the probability of clogging issues. The surface treatment, can fairly improve resolutions, but it requires additional steps thus sacrifices the advantages of 3-D printing technologies. Compared with an individual line, a gap with the same resolution is more complicated. For example, a 100 μm gap with 50 μm distortion was reported in [30] with a single layer. On the other hand, at a low frequency, the effect of conductor loss due to

the resistivity and surface roughness of the metals are small and not taken into account. However, the surface roughness is comparable with the skin depth of the metal in D-band. In addition, as the frequency increases to millimeter waves (mm-W), dimensions of circuit devices reduce in scale dramatically, resulting in a stricter requirement on the dimension.

Microstrip lines and conductor-backed coplanar waveguides (CBCPW) are the most commonly used and simple transmission lines in planar microwave circuit design. Historically (the interest in monolithic microwave integrated circuits (MMICs) in the 1970s and the prospects of performing on-wafer measurement by the use of CPWs, probes have been one of the major driving forces behind the integration of CPWs with microstrip lines. Furthermore, the CBCPW to microstripline transitions are commonly utilized for measurements and packaging of microstrip designs. Unlike other structures such as CPWG and stripline, they do not need vias and feature an exposed signal layer that simplifies component assembly. In section 2.1, AJP was assessed and it was demonstrated that the minimum value of the well-controlled width of a single silver line is 10 μm. The wavelength of D-band (110 GHz – 170 GHz) is from 2.7 mm to 1.7 mm, which is over 100 times of the minimum feature size of AJP and, thus, AJP is expected to be promising for D-band applications. This section demonstrates the capability of AJP in D-band applications by implementing various transmission lines and transitions. Development of conductor-backed coplanar waveguides (CBCPW), Microstrip lines and their transition by AJP is presented in this chapter. Lines with different lengths were designed, fabricated and measured. Measured attenuation and s-parameters are presented in this chapter. Results show that the attenuation loss of the fabricated lines is less than 0.3~0.5/dB at D band.

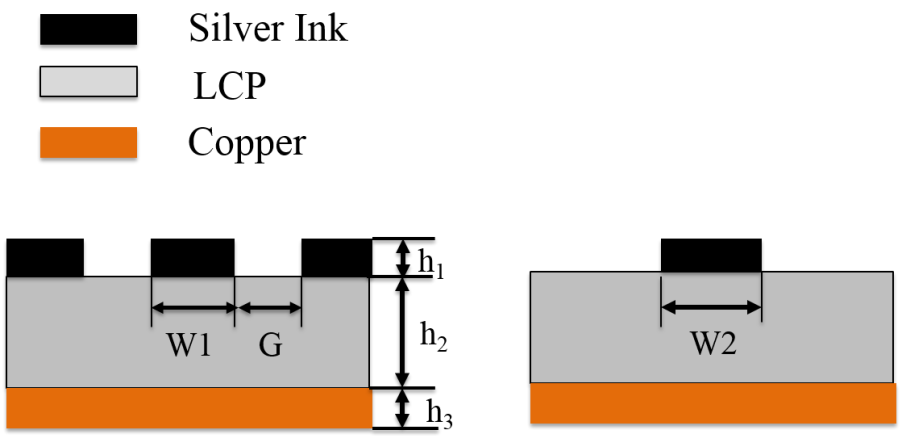


Figure 15. Cross Section View of the CBCPW and Microstrip Lines.

3.2 Design of D-band Interconnects

3.2.1 Via-less 60 Ω CB-CPW Lines, Microstrip Lines and Transitions

Figure 15 shows cross section view of CBCPW and microstrip transmission lines. The microstrip circuit has a signal line on the top of the dielectric substrate and a ground plane on the bottom. CB-CPW, similar as CPWG, has a coplanar layer with ground-signal-ground configuration on the top and another ground plane on the bottom and does not have a via connecting the three ground planes. Achieving a near 50 slot line impedance on a 2 mil thick LCP substrate requires that the width of the through slot line is about 100 μm and, the gap of the CPW is required to be less than 30 μm which falls below the limitations of standard printed circuit board (PCB) manufacturing processes or inkjet printing technology. Therefore, 60 ohm impedance CB-CPW lines are designed instead to be compatible for D band 75 μm probes' pitch, and also to reduce the dispersion effect at D band.

A standard 2 mil Rogers LCP with one side clad 9 μm copper was used as a ground plane in this work. Ten layers of silver ink were printed on the LCP substrate. For CB-

CPW, the desired Wgap was 30 μm, and the width of the center conductor was 70 μm. The length of lines 1, 2 and 3 were 1 mm, 2 mm and 3 mm, respectively. The practical parameters after fabrication are shown in Figure 5. Printed CPWG lines were designed as 1 mm long with Wgap =30 μm, Wsig = 70 μm, and Wgnd= 300 μm. The design parameters are calculated from ADS Linecalc and are shown in Table 4.

Table 4 Design parameters of CB-CPW and micostrip lines

Parameters	h_1	h_2	h_3	W_1	W_2	G
Values (μm)	4 μm	51 μm	9 μm	78 μm	100 μm	30 μm

The design of the CB-CPW to Microstrip transition is shown in Figure 16 which insists of a CBCPW portion, a transition portion and a microstrip portion. The two most important rules for the design of the transition are: impedance transformation and field transformation. The field transformation is realized by shaping the CBCPW side ground planes. For the transition portion, both signal line and the side ground planes are tapered gradually to transform both impedance and field to microstrip. In order to have a smooth transition from CB-CPW to microstrip, α shown in Figure 16 should be less than 40 degree. Full-wave simulations for various geometrical parameters were performed in HFSS to optimize the design regarding the operating bandwidth.

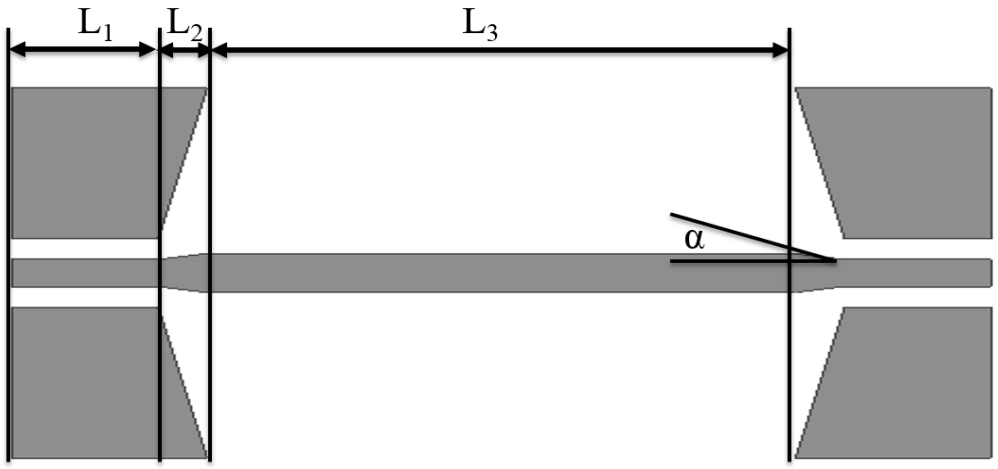


Figure 16 Structures of CB-CPW to microstrip line transition.

3.2.2 Design of TRL and TL Lines for Microstrip Loss Extraction

It is well known that the thru-reflect-line (TRL) calibration technique [31]-[33] has been widely used in microwave measurements. In [33], S-parameters of planar circuits are numerically extracted from full-wave MoM simulations. Compared with SOLT, TRL is able to obtain the parameters of error boxes and de-embed the measured port into arbitrary location as shown in Figure 17. There are four fictitious two-ports which are obtained from the thru, reflect, and line1 and line2 connections as indicated by the dashed box in Figure 17. With these measured S-parameters, the ones of DUT can be extracted. Calculation details are shown in [34]. In particular, the multiline TRL method of [31] offers a linear averaging strategy of noise and measurement uncertainties arising from imperfect connector repeatability and nonideal line standards.

It is necessary to design TRL lines in order to be consistent with NIST protocol. Equations (1)-(3) give the design guideline for the lengths of microstrip lines so that proper overlap of the delay are covered to provide adequate calibration coverage. F_{lower}, F_{upper} are the start frequency and the end frequency of the interest respectively and F_{90} is the center of the valid frequency range for a given delay line.

$$F_{lower} = \frac{20\ C}{360(L_{in} - L_{thru})\sqrt{\varepsilon_{eff}}} \quad (1)$$

$$F_{90} = \frac{90\ C}{360(L_{in} - L_{thru})\sqrt{\varepsilon_{eff}}} \quad (2)$$

$$F_{upper} = \frac{160\ C}{360(L_{in} - L_{thru})\sqrt{\varepsilon_{eff}}} \quad (3)$$

Two calibration lines were designed to provide a 90º shift at different frequencies of the measurement bandwidth, while keeping the phase shift of each line above 50º over the entire bandwidth. The calibration plane was set to the edge of the microstrip end of the transition as AA' and BB' in Figure 18 and the required length of the TRL lines set is listed in Table 5.

Table 5 TRL lines length

Line Type	Line Length (μm)
Thru	0
Delay Line1	300 μm
Delay Line 2	400 μm
Measured Line	2000 μm

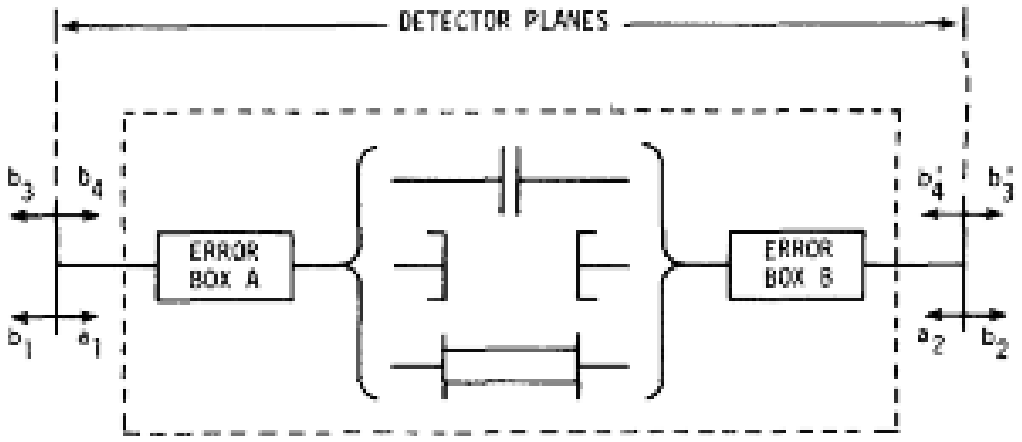


Figure 17. The fictitious two-ports, from which the parameters of "error boxes" A,B are ultimately obtained, and are formed from a "thru, reflect and line" connection. [33]

In this dissertation, a novel two-tier de-embedding scheme based on the above described TRL procedure is introduced from [34] and applied. This scheme is applicable to a range of configurations where the error adapters are either geometrically or electrically symmetrical in regard to the midpoint in the thru standard while TRL is valid in a broader application (including asymmetrical applications).

First, define the thru standard in Figure 18 as a cascade connection of two transitions in a back-to-back configuration and the line1 standard as connection of two transitions of connected through a length of microstrip line. The chain transmission matrices of the thur $(T)_{thru}$ and line $(T)_{line}$ standards can now be expressed by [34].

$$(T_{line1}) = (T_{trans}) \cdot (T_{delay}) \cdot (T_{retrans}) \tag{4}$$

$$(T_{thru}) = (T_{trans}) \cdot (T_{revtrans}) \tag{5}$$

$$(T_{trans}) = \frac{1}{s_{21}} \cdot \begin{pmatrix} 1 & -s_{22} \\ S_{11} & S_{21}^2 - s_{11}s_{22} \end{pmatrix} \tag{6}$$

$$(T_{retrans}) = \frac{1}{s_{21}} \cdot \begin{pmatrix} 1 & -s_{11} \\ S_{22} & S_{21}^2 - s_{11}s_{22} \end{pmatrix} \tag{7}$$

$$(T_{delay}) = \begin{pmatrix} e^{-\gamma L_L} & 0 \\ 0 & e^{\gamma L_L} \end{pmatrix}, \tag{8}$$

where S_{11}, S_{22} and S_{21} denote the S-parameters of the transition of Figure 18. In the derivation of (6)-(8), the reciprocity of the transition is taken into account by $S_{12} = S_{21}$ and γ is the complex propagation constant while L_L represents the length of the mcirostrip line between the two transitions, which is 0 mm for the case of the thru standard and 1mm for the line1.

The thru and line standards (4) can be represented in terms of the overall s-parameters of the thru and line1 as

$$(T_{thru}) = \frac{1}{\tau}\begin{pmatrix} 1 & -\rho \\ \rho & \tau^2 - \rho \end{pmatrix} \tag{9}$$

$$(T_{line1}) = \frac{1}{\tau'}\begin{pmatrix} 1 & -\rho' \\ \rho' & \tau'^2 - \rho' \end{pmatrix} \tag{10}$$

Where ρ and τ represent the reflection and insertion losses of the thru standard, while ρ' and τ' stand for the reflection and insertion losses the line standard. Substituting (6), (7) in to (3), (4) and obtaining

$$\rho = \frac{S_{11} + S_{22} \cdot (S_{21}^2 - S_{11} \cdot S_{22})}{1 - {S_{22}}^2} \tag{11}$$

$$\tau = \frac{S_{21}^2}{1 - {S_{22}}^2}. \tag{12}$$

And similarly

$$\rho' = \frac{S_{11} + S_{22} \cdot (S_{21}^2 - S_{11} \cdot S_{22}) \cdot e^{-2\gamma L_L}}{1 - {S_{22}}^2 \cdot e^{-2\gamma L_L}} \tag{13}$$

$$\tau' = \frac{S_{21}^2 \cdot e^{-2\gamma L_L}}{1 - {S_{22}}^2 \cdot e^{-2\gamma L_L}}. \tag{14}$$

So the three independent unknown parameters S_{11}, S_{22} and S_{21} can be determined

$$s_{11} = \frac{\tau \cdot \rho' - \rho \cdot \tau' \cdot e^{-\gamma L_L}}{\tau - \tau' \cdot e^{-\gamma L_L}} \tag{15}$$

$$S_{21}^2 = \frac{\tau - \tau' \cdot e^{\gamma L_L}}{\tau - \tau' \cdot e^{-\gamma L_L}} \tag{16}$$

$$S_{22}^2 = \frac{\rho - \rho'}{\tau - \tau' \cdot e^{-\gamma L_L}}$$

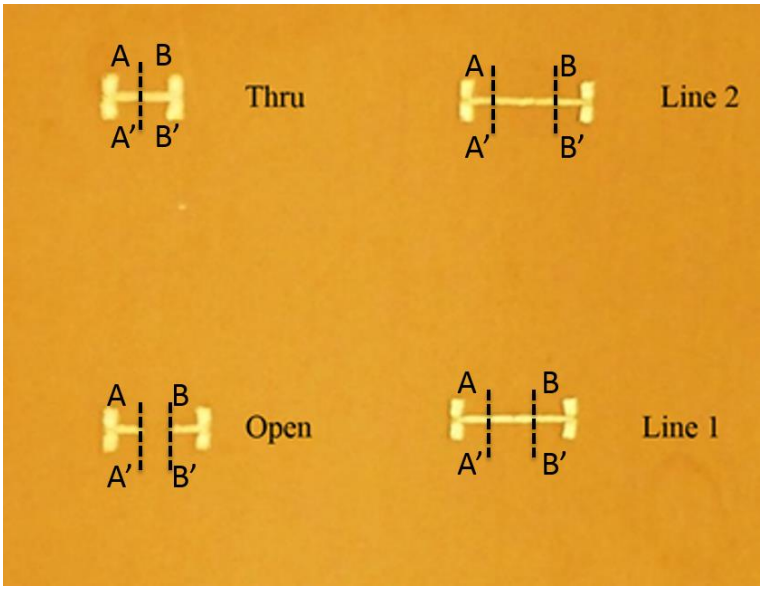
Thus, by measuring (T_{thru}) and (T_{line}) for the thru and line1, the scattering parameters of the transition can be obtained.

3.2.3 Fabricated Samples and Measurement

The actual fabricated samples are shown in Figure 18. All D-band transmission lines were printed on a standard 2 mil Rogers LCP with one side clad 9 μm copper which was used as a ground plane in this work. Ten layers of silver ink were printed on the LCP with a 150 μm nozzle on LCP substrates. The distance from the nozzle to the substrate is 4 mm. Substrate temperature was controlled at 50 °C in order to properly control the resolution. The curing temperature is gradually increased to 200 °C for 1 hour. The dimensions of the samples from the design and the fabrication are shown in Table 6.

Table 6 Fabrication error of the sample

Parameters	h_1	W_1	W_2	G	L_1	L_2	L_3 (Thru.)
Design (μm)	3.5	78	100	30	200	100	1000
Fabricated	3.4	79	96	28	196	102	1000
Fabrication Error	2.8%	1.3%	4.0%	6.7%	2.0%	2.0%	0.0%



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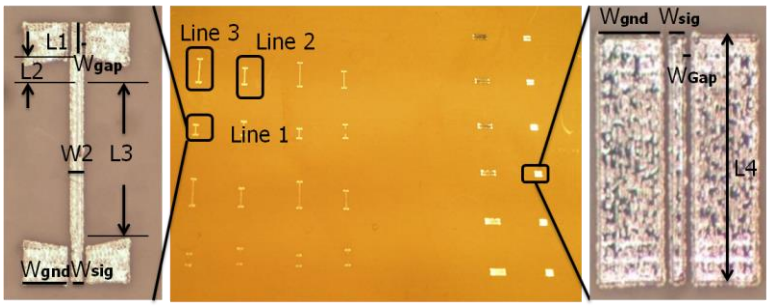


(b)

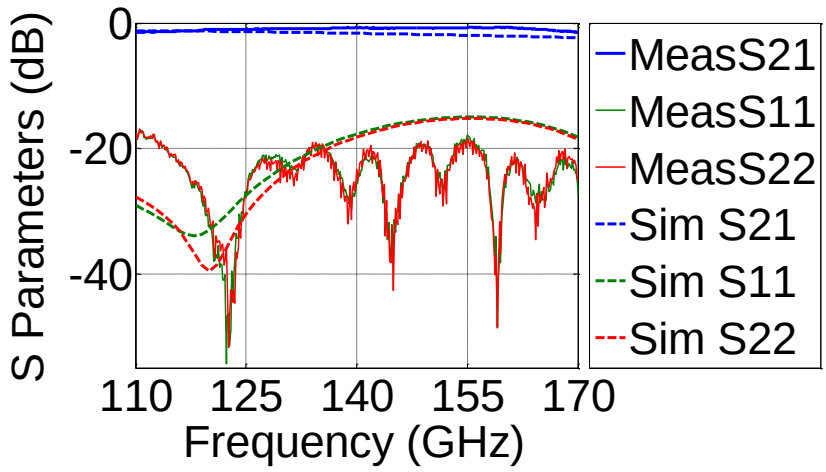
Figure 18. (a) Fabricated CB-CPW to microstrip lines sets. (b) Fabricated 28 samples in a big panel that only takes 10 mins.

An Agilent E8361C vector network analyzer with N5260A (mm-Wave controller) and V06VNA2 (mm-Wave Test Heads) were used to measure the transmission lines in the D-band (110 GHz-170 GHz). 75 µm pitch Cascade Micro Tech Infinity D-band probes were used. An LRRM calibration was performed on Cascade 138-356 ISS. For the D band CB-CPW-to-microstrip transition, the loss is the combination of the CPWG pads, transition and the microstrip line.

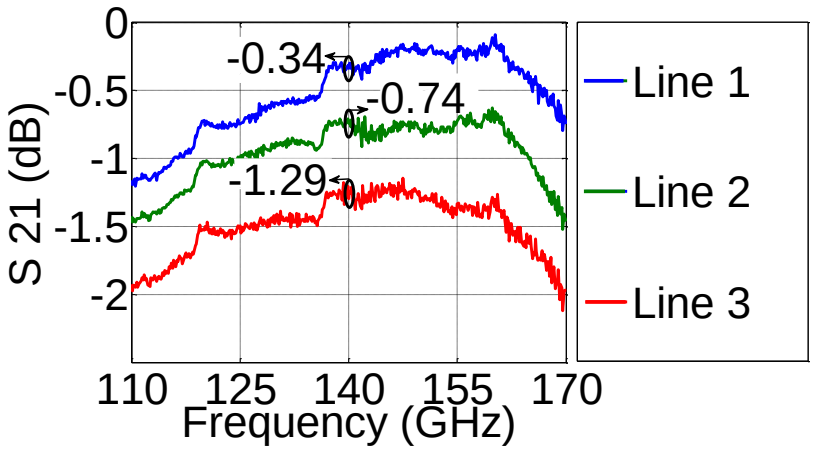
The total loss α_{tot} is composed of conductor loss α_c, dielectric loss α_d and radiation loss α_r as shown in equation (2). Conductor loss was subtracted through Agilent's LineCalc software using the conductivity corresponding to ten printed layers and heat sintering at

200 °C. The dielectric loss can be related to the loss tangent. The radiation loss is not negligible at D band and becomes dominant when the frequency increases. The total effects were simulated in HFSS with 6 μm thick of the silver ink with 2 μm surface roughness model.

The measured results are shown in Figure 19. It is found both of the transition are wideband through the whole D-band. Using the TL calibration methods described in 3.2.2, the loss of the microstrip lines was approximately 0.35 dB/mm at 110 GHz and 0.51 dB/mm at 170 GHz. This is close to the best reported D-band microstrip lines made by photolithography process with copper traces [5] (0.1755 dB/mm) and 0.24 dB/mm on 2 mil LCP [7], and is 1/10 of the loss of the inkjet printing lines (-3 dB/mm at 100 GHz) [1]. The CPWG lines shown in Figure 18 (b) have a 0.28 dB/mm insertion loss at 110 GHz and 0.6 dB/mm at 170 GHz. The additional loss can be attributed to the thinner printed conductive ink along the edges of the CPW slots.



(a)



(b)

Figure 19. Measured S-Parameters of CB-CPW and microstrip to CPW transitions. (a) Comparison of simulation and measurement of line 1 and line 2. (b)Comparison of simulation and measurement of CPWG Insertion loss of line 1, line 2, line3.

CHAPTER 4

A HYBRID LNA CIRCUIT ON A FLEXIBLE ORGANIC SUBSTRATE IMPLEMENTED BY AJP

4.1 Introduction of Flexible Organic Materials

Recently, flexible organic light-emitting diodes (OLEDs) have attracted a lot of interest because of their potential in lighting and the generation of flexible displays [35]-[37]. Besides glasses, numerous research examples demonstrate OLED on flexible substrates. PET (Melinex), Polyimide (Kapton), PES (Sumilite) and other materials are widely used as flexible organic substrates.The LNA presented in this work is packaged on Teonex ® PEN film that is a DuPont's biaxially oriented polyethylene naphthalate (PEN) film. This new product range has been developed specifically to meet customers' needs for cost effective films with performance between that of polyethylene terephthalate (PET) and polyimide. Compared with PET that dominates low cost flexible substrates, Teonex PEN has an excellent dielectric strength (25% greater than PET) and greater hydrolysis resistance. Compared with cheap papers [38], PEN is a low loss substrate for high frequency devices. In addition, it is much lighter than PC boards and transparent. Preliminary research on RF applications such as antennas, waveguides, ring oscillators and so on, has been performed based on PEN [38]-[40], but little research has been done to analyze the loss of the materials at microwave bands and no literature shows any low noise amplifier designs. In this chapter, a low noise 2.45 GHz amplifier was designed, fabricated and tested.

First, the PEN's dielectric constant was characterized using microstrip lines and T resonators. The dielectric constant and the loss tangent was extracted from these designs. The dielectric constant is 2.12 at 2.4 GHz while the loss tangent was 0.007.

4.2 Active Microwave Circuit Implemented by AJP

An LNA was designed based on a PEN substrate at 2.4 GHz. Optimization among the noise figure (NF), input matching and the power gain was performed and simulated by ADS. The schematic of the design is shown in Figure 20. The Gummel-Poon model of the NPN transistor BFP540 from Infineon was commercially available at the vendor's website. The LNA was designed in an inductive degeneration common emitter configuration. The input impedance seen into the NPN transistor is

$$Z_{in} = j\omega L_e + \frac{1}{j\omega C_{be}} + 2\pi f_T L_e. \quad (17)$$

A transmission line was used at the emitter serving as an inductor (L_e) that represents the packaging degeneration. f_T is the unity-gain frequency and C_{be} is the capacitance between the base and the emitter. In this design, an input impedance of (34.702+j×11.734) and an output impedance of (36.875+j×25.890) were chosen. Therefore, the input matching condition and the noise matching condition can be simultaneously achieved, as shown in Equation 18.

$$Z_s = Z_{opt} = Z_{in}^*. \quad (18)$$

From the model of the transistor under V_{ce}=5 V and I_c= 10 mA, the simulated minimum noise figure was 1.8 dB with a power gain of 13.7 dB. One important design

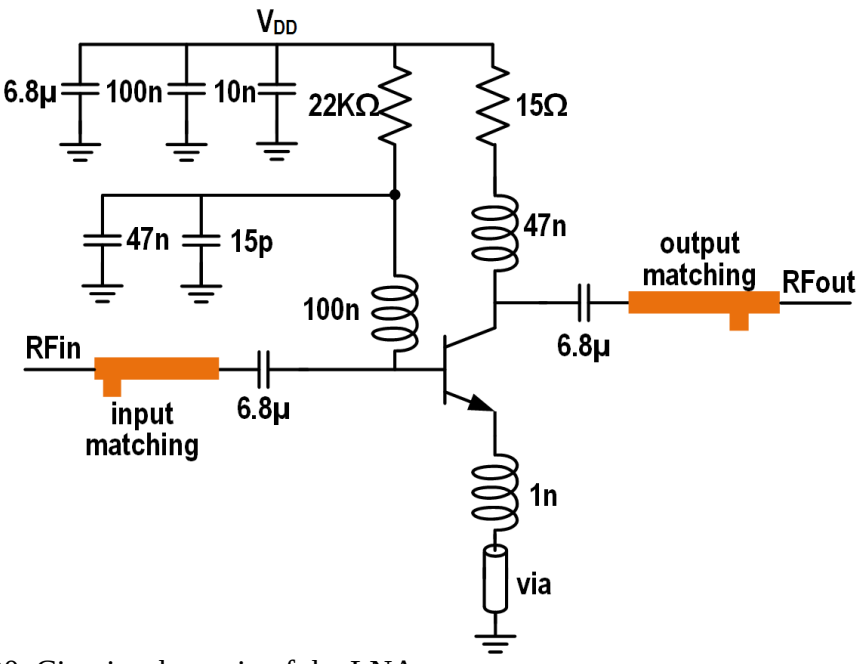


Figure 20. Circuit schematic of the LNA.

aspect is to make sure the LNA unconditionally stable, which can be characterized using the stability factor K. The inductive emitter degeneration also helps to stabilize the LNA to achieve K >1.

A 250 µm PEN film (TENOX Q51 untreated film from Dupont) with 50 µm copper tape on both sides was used as the starting substrate material. The top side copper taps form the matching network and bias circuit while the bottom side copper taps serve as the ground. Since the resolution was limited by the copper tap, 20 Ω microstrip lines with 3 mm width were used to design the matching network. The total dimension is 115 mm x 65 mm. The fabricated LNA is shown in Figure 21. Photograph of the fabricated LNA..

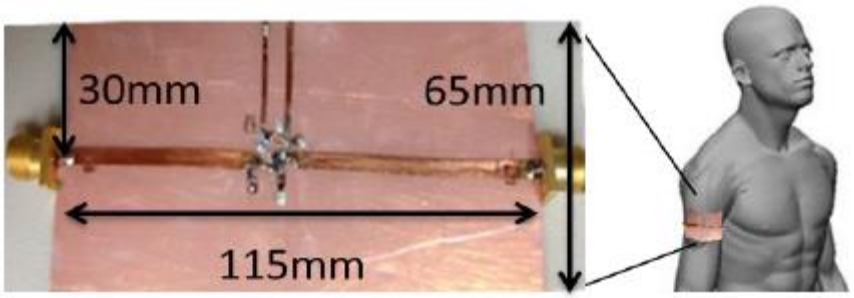


Figure 21. Photograph of the fabricated LNA.

The S-parameters for the LNA were measured using an Agilent VNA (8510C). A SOLT calibration was performed. **Error! Reference source not found.** shows the easurement and simulation results. Mechanical tests on conforming the LNA to a curved surface were also performed. The maximum stretching of the device reached up to 40cm as shown in the Figure 26 without any plastic deformation or damage to the device or the SMA connectors. The curvature of the LNA has caused a slight increase of S_{11}. The highest S_{11} was observed when the curving radius reached up to 40 cm. However, the return loss still resonates at 2.45 GHz without much shift. When the LNA was attached to a human's arm with curving radius of 40 cm, a resonant shift of 100 MHz from 2.45 GHz to 2.3 GHz was observed.

In Figure 23, the measured gain is 13.8 dB which agrees well with simulation at 2.45 GHz. From the simulation, the noise figure is 1.8 dB and OIP3 is 24 dBm. For an input return loss better than 10 dB, the bandwidth is 500 MHz from 2.05 GHz to 2.55 GHz.

The noise figure was measured using Agilent PXA. The setup is shown in Figure 22. A noise source was connected from the RF input of the LNA and the output of the LNA connected to the PXA. The LNA was attached to a 120 cm curvature cylinder. With a DC power consumption of 65 mW, the noise figure was measured and shown in Figure 24. At

2.41 GHz, the noise figure is 2.7 dB compared with a 1.8 dB simulated value. The PEN substrate is a flexible organic material. The conformal condition for its future application in the area of wearable devices was assessed and the measurement results of S_{11} is shown in **Figure 26**.

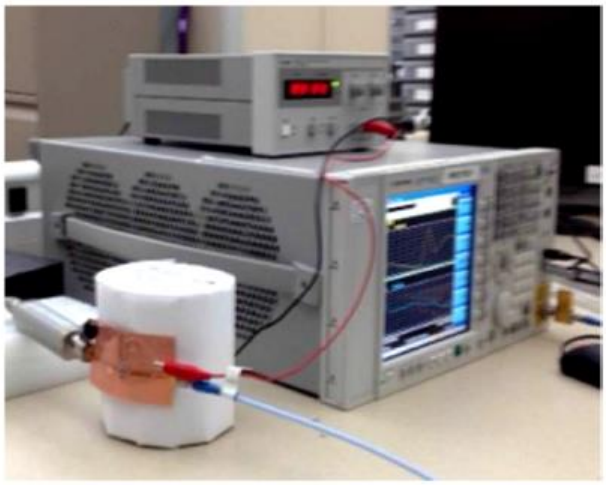
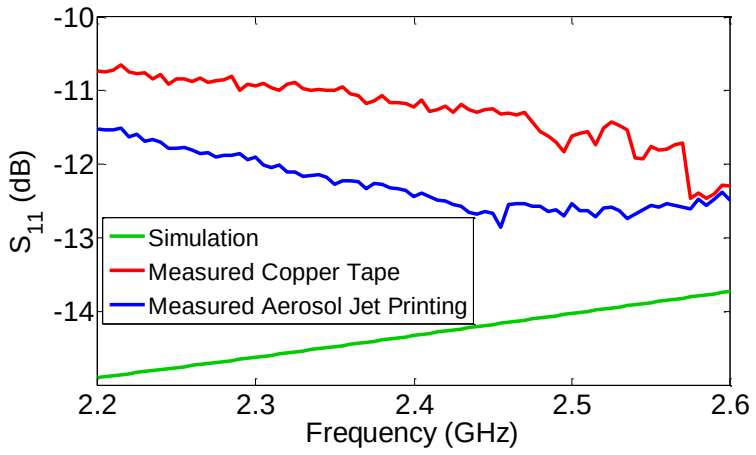
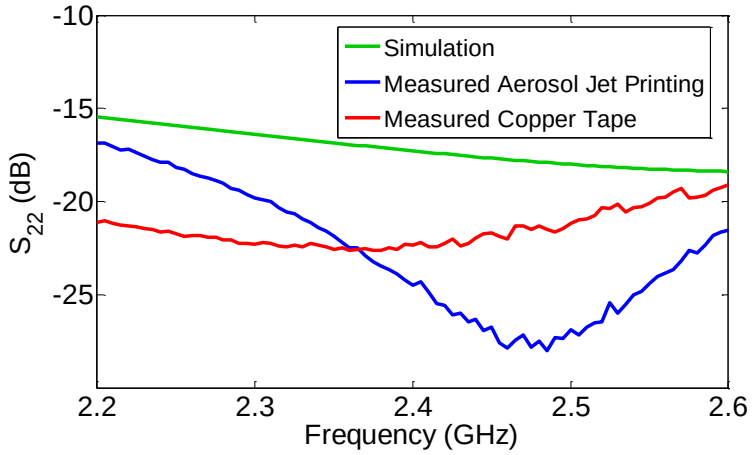


Figure 22. Photograph of the measurement setup.



（a）



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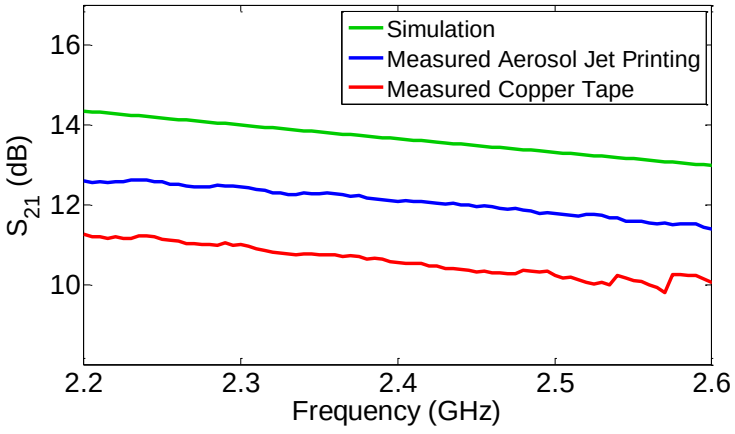


(c)

Figure 23. Simulated and measured S-parameters.

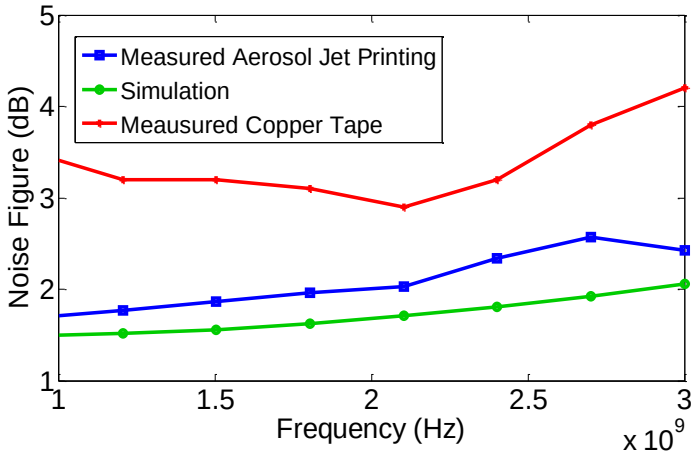


Figure 24. Simulated and measured noise figure.

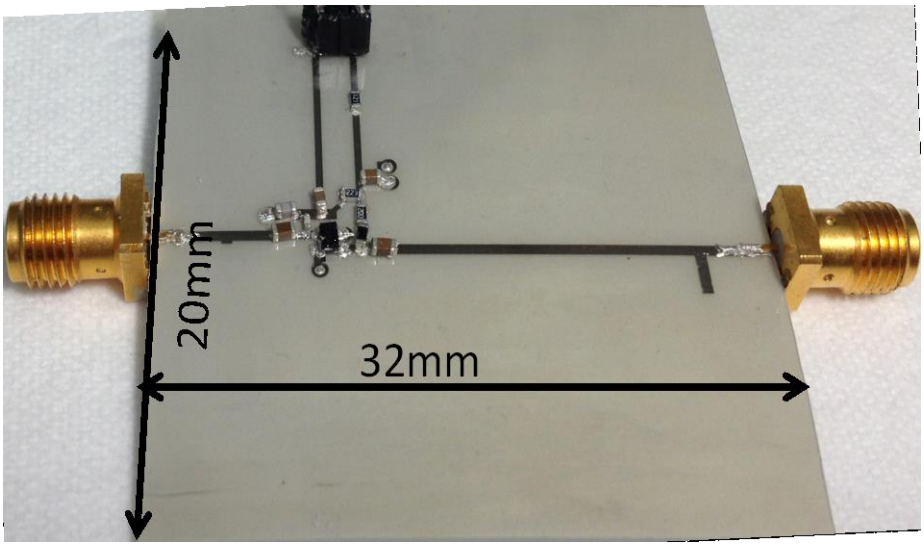


Figure 25. The LNA sample printed by AJP

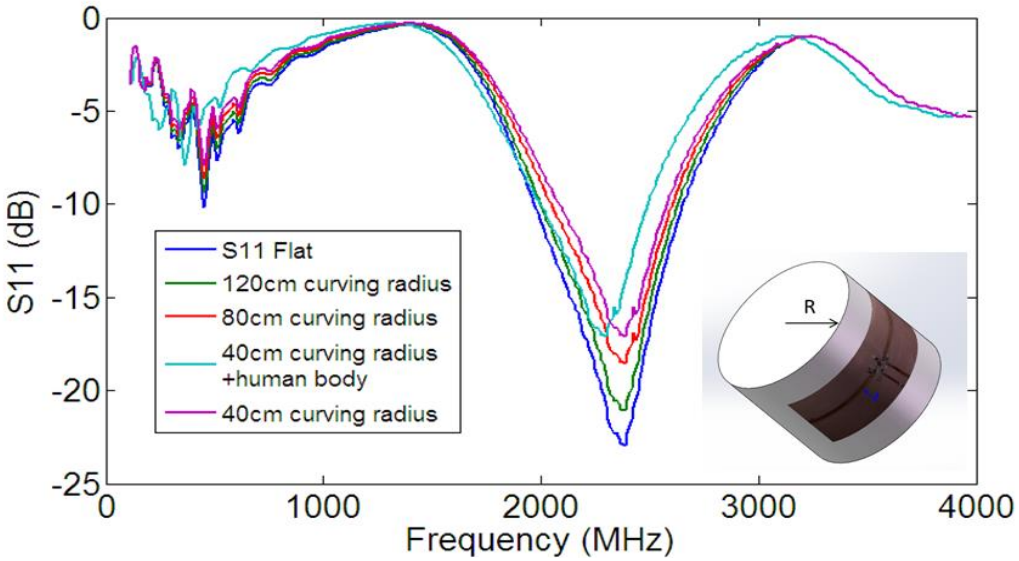


Figure 26. The response of S_{11} on the conformal conditions and human body's effects.

CHAPTER 5

MULTILAYER PRINTING BY AJP

5.1 Background of Multilayer Interconnects and Packages

3-D packaging technologies for multichip modules are necessary in high-frequency communication systems since the current 3-D ICs are promising for the heterogeneous integration of different technologies (logic, memory, RF, analog etc.) which are enabled by high performance and compact System-in-Package (SiP) or System-on-Package (SoP). To better understand the extent of LCP packaging capabilities at microwave and mm-wave frequencies, several packaging methods have been explored and a method of RF/mm-wave design preferred from many viewpoints is a multi-layer structure [43]-[45]. The conceptual drawing of the full 3D printed multichip module is shown in Figure 27. The circuit vertically integrated with IC chips embeds traces and vias in which way the whole multi-chip module can substantially reduce size but typically place a huge fabrication challenge on 3-D printers.

A good interconnect plays an important role in a package design, especially for SoP designs. It is desired to provide good field confinement, proper impedance matching and broadband bandwidth. In addition, a vertical transition usually requires embedded vias with a high height aspect ratio. So far, few literature report the multilayer transition implemented by digital printing technique mainly due to constraints imposed by printers. For instance, to the best knowledge of the author, the minimum fabricated vias by inkjet is larger than 100 μm, the stacking layers are thinner than 20 μm. A 100 μm gap with 50 μm distortion was reported in [46] with a single layer. Stacking of multiple metal layers without distortion to reduce the loss of the transmission lines and avoid mismatch was not demonstrated.

This chapter provides a comprehensive investigation on the capability of multilayer printing for RF circuits and signal integrity performance that can be achieved. Special printing techniques are utilized to minimize RF parasitic effect incurred through the package interconnects. The aim is to offer high performance integration for low-cost and lightweight applications.

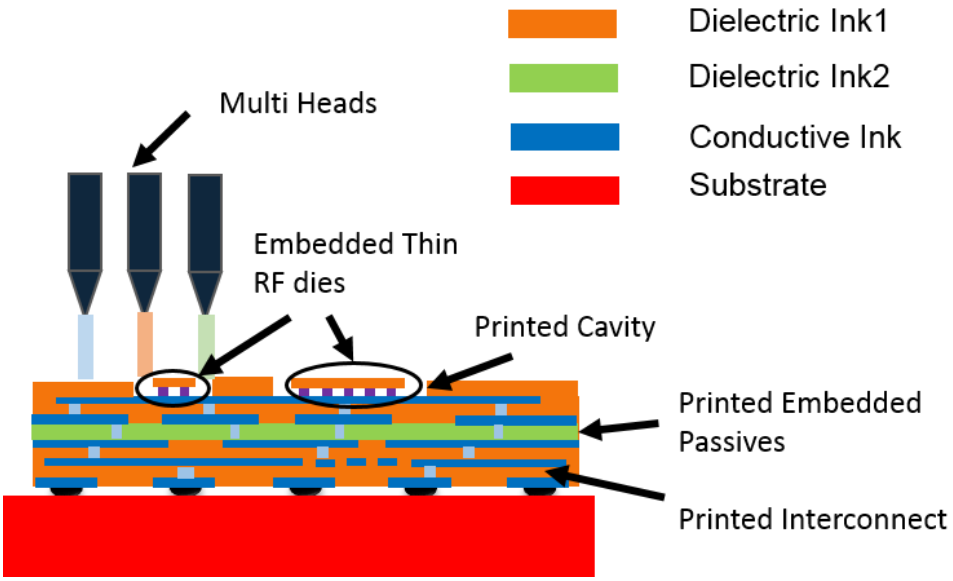


Figure 27. Conceptual diagram of SoP topology achieved by 3D printing.

5.2 Multilayer Transmission Lines on Different Substrates by 3-D Printing

Three types of 50 ohm coplanar waveguides with ground planes were designed as shown in Figure 28. For type 1 and type 2, the host substrates were 2 mil Rogers ULTRALAM®3850 (LCP) with one side copper clad layer used as a ground plane. As shown in Figure 28, in type 1, 8 μm of silver ink was printed on LCP directly. In type 2, a 10 μm thick 2 cm x 3 cm polyimide layer printed on LCP followed with 8 μm printed silver ink on it. Afterwards, a completely 3-D structure which can be achieved on any host substrate is demonstrated. In type 3, a 1 mm glass host was used. First 10 layers of silver ink were deposited (for the ground plane) which amounted to approximately 7 μm, then 15

μm polyimide was printed above the silver ink. Finally, another 10 layers of silver ink were stacked on the top of the polyimide.

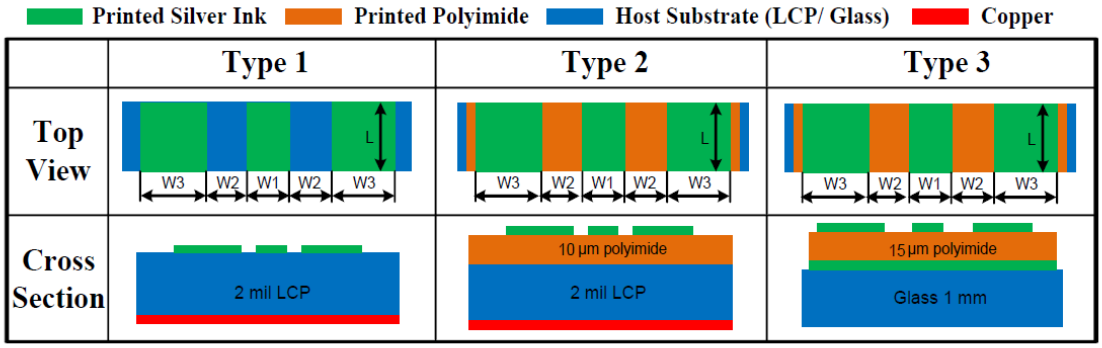


Figure 28. Designed 3-D coplanar waveguides.

The designed and measured parameters are shown in Table 7:

Table 7 Design parameters of CPWG lines

	Design	Meas #1	Meas #2	Design on Polyimide	Meas # 3
Z_0	50 Ω	53 Ω	59 Ω	50 Ω	48 Ω
W_1	138 μm	140 μm	140 μm	35 μm	37 μm
W_2	50 μm	48 μm	45 μm	70 μm	65 μm
W_3	300 μm	301 μm	301 μm	500 μm	502 μm
L	2 mm	2 mm	2 mm	1.5 mm	1.5 mm

The fabricated samples are shown in
Figure 29. The CPW line in
Figure 29 (d) shown under a microscope forms a 30±2 μm gap without shorting the signal line and the ground. An Agilent 8517B vector network analyzer was used to take all the scattering-parameter measurements. 250 μm pitch GSG Picoprobes were used. An LRRM

calibration was performed with Wincal to remove cable and probe losses. A good calibration was achieved with a slight variation of 0.01 dB for the S_{21} measurement of the thru standard. The measured scattering parameters of the CPWG lines are shown in Figure. From the measurements, good matching under 50 GHz was achieved for all the three types. The insertion loss of type 1 was 0.08 dB at 100 MHz and increased to 1.3 dB at 50 GHz. Compared with the type 1, the insertion loss of the 2 mm type 2 lines increased approximately 0.1 dB after 10 μm polyimide deposited on LCP. For the completely printed CPWG of type 3 in Figure (c), a 0.7 dB insertion loss at 50 GHz was found.

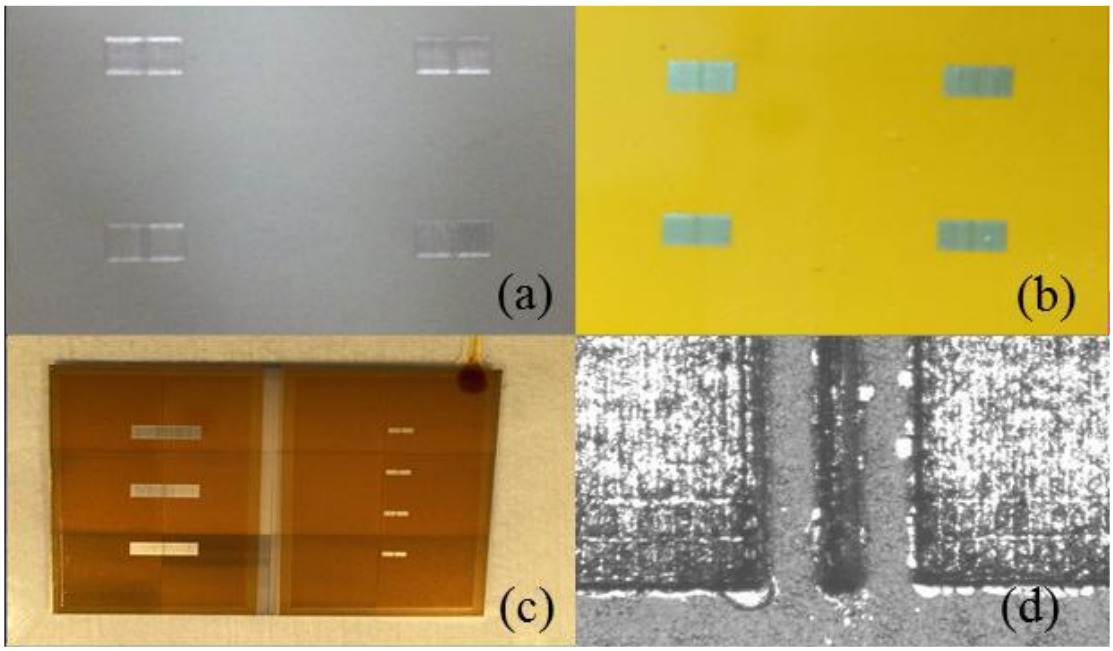
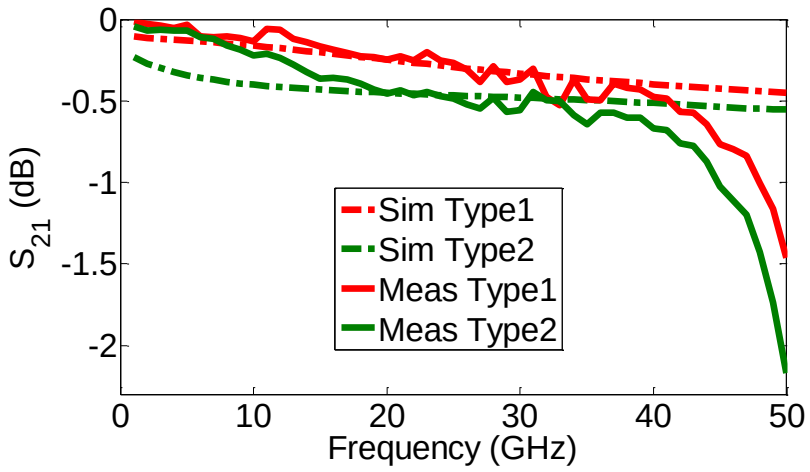
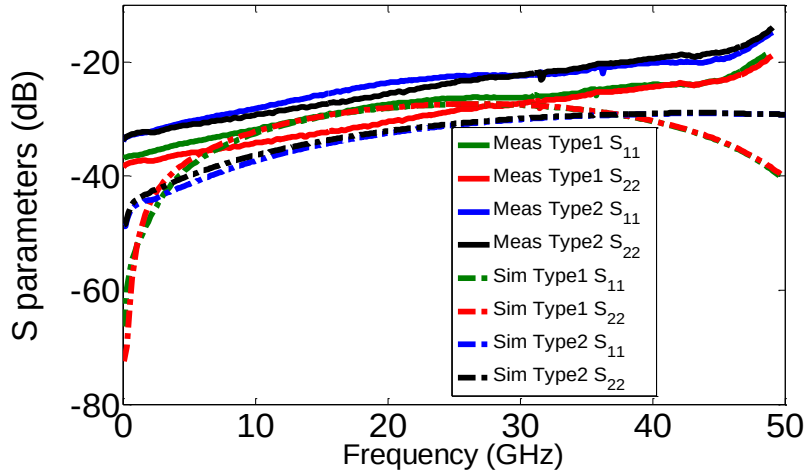


Figure 29. Fabricated CPWG samples by aerosol jet printing system: (a) printed silver ink on 2 mil LCP as type 1, (b) the same dimension as type 1 with an additional 10 μm polyimide layer on LCP (c) printed metal-polyimide-metal 3-D structures as type 3 on the glass. (d) microscope image of the printed CPW lines.



(a)



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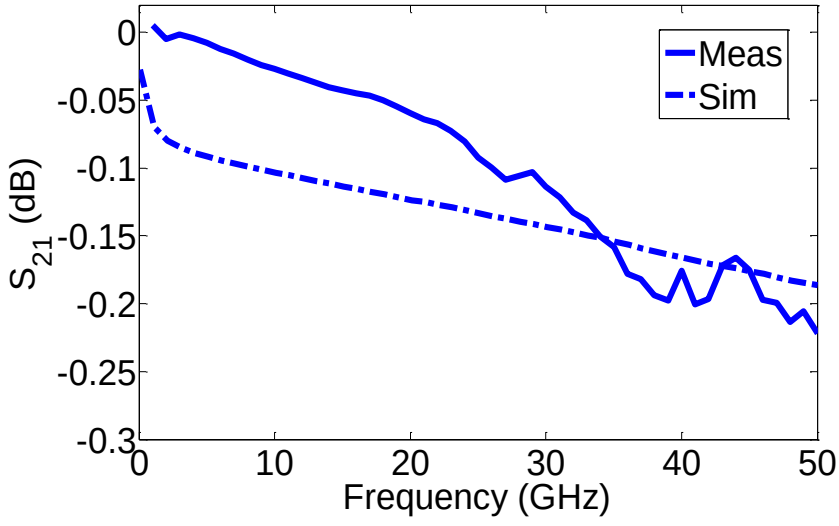
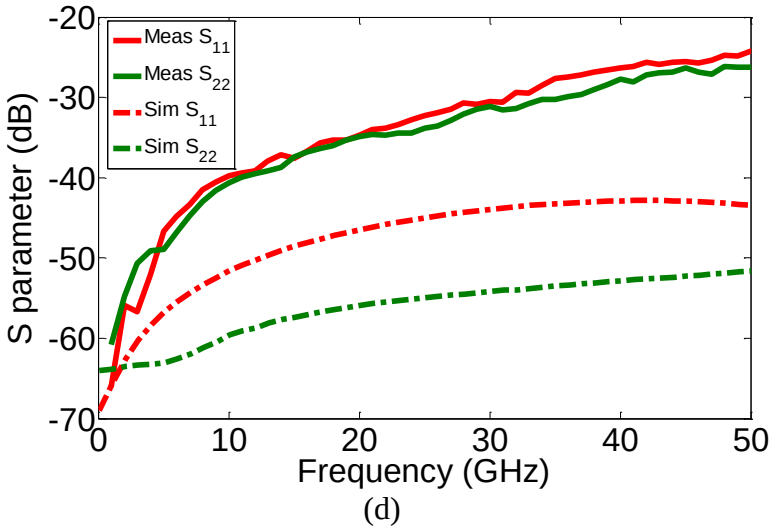


(c)

Figure 30. Simulated and measured S-parameters of the three types of printed samples.



(d)

Figure 30. Continued.

5.3 Transition with Embedded Vias

The 3-D packaging technologies for multichip modules are extremely important in mm-wave systems. With the development of advanced MMICs, it is very promising to achieve the heterogeneous integration of different technologies (logic, memory, RF, analog, MEMS etc.) which are enabled by high performance and compact System-in-Package (SIP) or System-on-Package (SOP) solutions. This requires a highly accurate true 3-D fabrication technology for RF/mm-wave circuits and, thus, an extensive effort to make vertical interconnections [11]-[13]. Nevertheless, designs at higher frequencies, especially at mm-wave frequencies, suffer from the strict limitations of the 3-D printing on acceptable tolerances. To date, the minimum line width of inkjet printing technology is around 25 μm due to the restriction of nozzle technologies. However, the dimension of the nozzle faces a bottleneck to be further reduced. On the other hand, to be useful for the compact multilayer circuits with vertical interconnection, 3-D printing technologies must allow continuous manufacturing of all circuit components by successive ink solution deposition plus printing steps in the same environment. Fabrication difficulties lie in the formation of via-holes, substrate thickness uncertainty and misalignment that restrict the current 3-D printing

technologies for single layer interconnection [70]. Through traditional fabrication methods, vertical vias through the board are commonly enabled by drilling. Few works have yet demonstrated a comprehensive research on the vertical interconnection by 3-D printing. M. Liang et al. reported a microstrip line structure with the vertical transition through vias with the diameter of 2 mm [71]. Lopes et al. fabricated a 3D 555 timer circuit with multi-dimensional interconnections [72] where the vias were manually filled. At present, printed vias with a diameter of smaller than 500 μm, whereby an all-printed multilayer circuit is connected, are challenging while via metallization also brings increased difficulty.

In all, to be competitive with traditional fabrication method for RF/mm-wave applications, especially for the future 5G communication systems, 3-D printing technology needs to satisfy the following features: planar fine pitch size of less than 20 μm to realize complex structures; ability to stack up multilayers with thickness accuracy up to 10 μm; maintaining alignment less than 10 μm; and realizing embedded vias to achieve vertical transitions. All of these requirements place fabrication challenges on 3-D printing technologies. Although some reports have solved the first two of the aforementioned fabrication issues, so far no other literature has yet addressed all of these stringent requirements [73]-[74]. Therefore, highly accurate and cost effective fabrication of mm-wave circuits by 3-D printing technology is still very challenging.

Typically, there are three ways to implement a transition shown in Figure 31 : (1) transition using a via-hole, (2) aperture-coupled transition, and (3) cavity-coupled transition. The via-hole structure typically generates large parasitics. In order to alleviate the parasitic effects, [70] presented a design that used stepped vias and embedded air cavities to tune transitions for 60 GHz ISM band. A simulation for a wide frequency range from DC to 30 GHz vertical transition was achieved using via fencing based on LTCC but there was a frequency shift between the simulation and measurement which was expected to be caused by misalignment and fabrication tolerance. The structure in Figure 31 (b), it

works like a two-pole band pass filter circuit and no physically design guidelines have been reported so far. The structures in Figure 31 (c) can be considered as a modification of the structure in Figure 31 (b) by thickening the common ground plane. The via-walls inescapably increase the manufacturing difficulties for high-frequency applications. Both these two structures are more challenging for the fabrication and thus we mainly consider the via-hole structure here.

In this thesis, we propose to apply the AJP for vertical CPW-Stripline transitions for the first time. A modification transition configuration of the via-hole transition shown in Figure 31 (a) has been chosen for easy fabrication and prototyping.

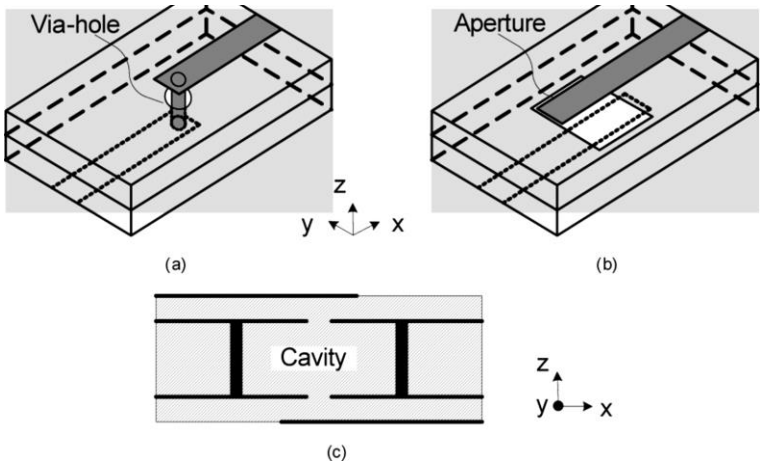


Figure 31. (a) Via-hole transition, (b) aperture coupling transition, and (c) cavity coupling transition.

5.3.1 Designs and Fabrication

Interconnect techniques play a key role in microwave/mm-wave modules, especially as the frequency of operation increases. At higher frequencies, transmission lines and interconnection schemes that minimize crosstalk, insertion loss and radiation while maintaining wideband performance are required. As one of the most important transmission lines, stripline provides better performance, in terms of higher isolation and less crosstalk and radiation than its counterparts, e.g. microstrip line and coplanar

waveguide, attributed to its non-dispersive nature based on the TEM mode and shielded structure. Therefore, it is often required in the multilayer routing for microwave circuits. However, it correspondingly gives rise to tighter manufacturing tolerances for a dense design with smaller traces. Stripline samples and vertical interconnections are designed here to demonstrate the superior performance by AJP technology.

In order to measure the samples with RF probes, a coplanar waveguide (CPW) to Microstrip (MS) to Stripline (SL) transition is designed. Multiple layers are stacked for

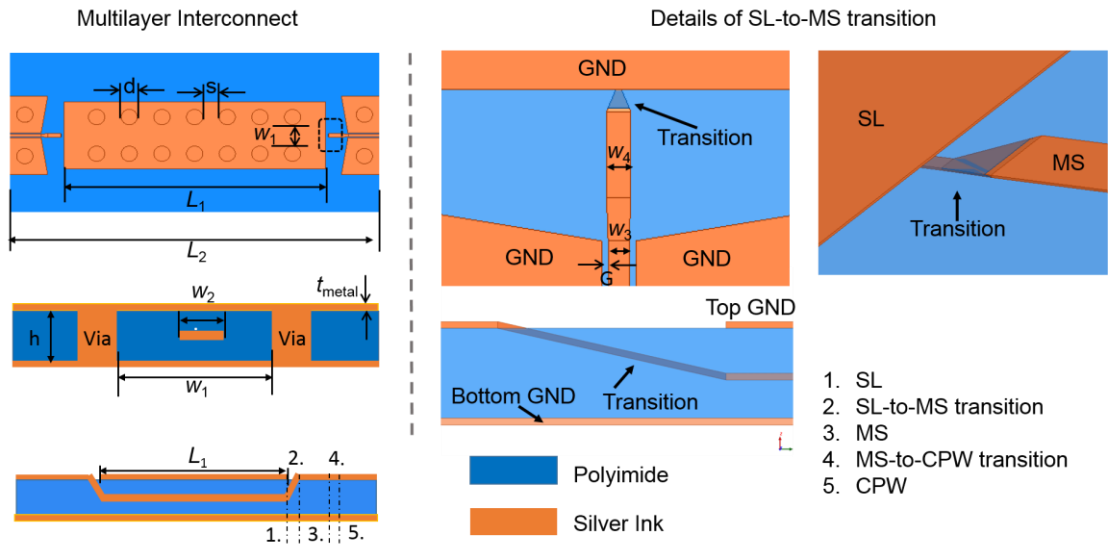


Figure 32. The structure of the multilayer interconnect and the transition.

interconnect routing and the structure is detailed in Figure 32. The whole structure consists of five layers, including two transitions: CPW-to-MS and MS-to-SL. The dimension values of CPW, MS and SL are calculated by the LineCalc in ADS. In the CPW-to-MS transition section, the width of the CPW signal strip (90 μm) is gradually increased to match the width of the microstrip line (110 μm). At the same time, the gap between the ground planes and the signal line is widened to retain a 50 Ω characteristic impedance to avoid sharp discontinuities and minimize reflections [77]. This transition is a planar transition with the signal line continuing on the same plane. To provide vertical interconnection, the MS-to-

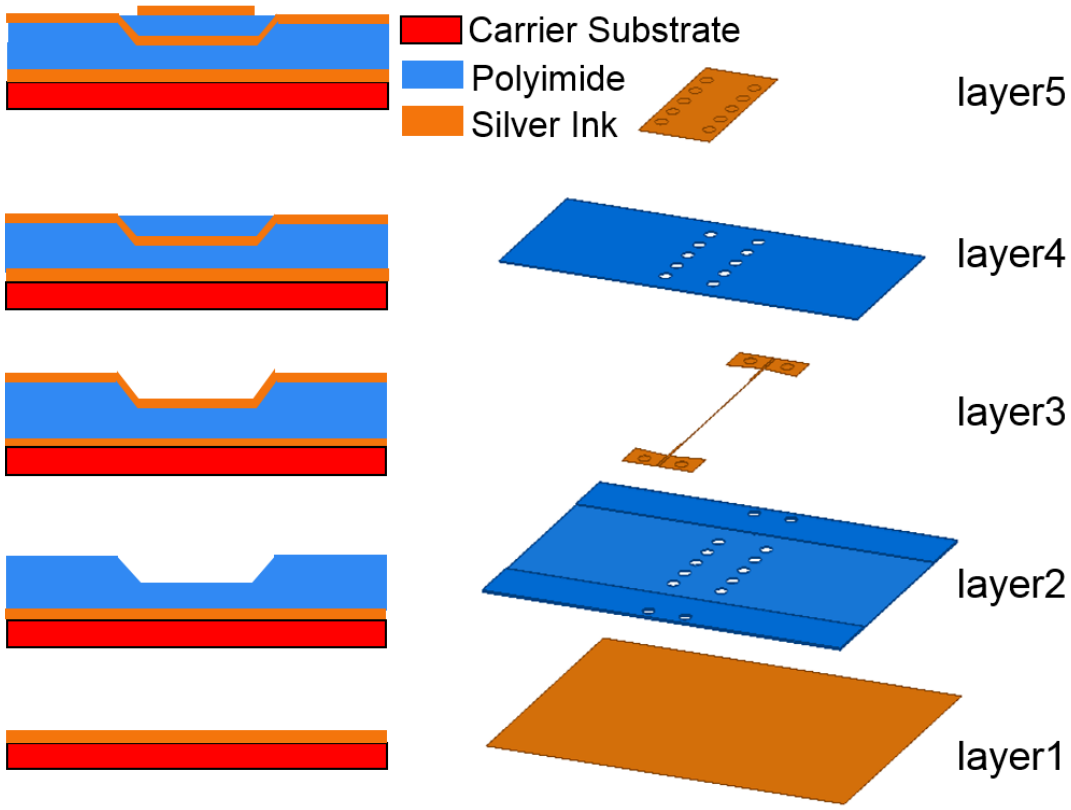


Figure 33. Fabrication process of the multilayer interconnect.

SL transition is developed. Instead of the 90 degree vertical via conventionally deployed [67], [68], the proposed one in Figure 32 (on the left) consists of an inclined metal sheet tapering from 110 μm (the width of the MS signal line) to 19 μm (the width of the SL signal line).

The fabrication process is described in Figure 33. First, a silver ink layer as layer 1 was printed as the bottom ground followed by layer 2 constituting polyimide. The two sides of layer 2 were 40 μm thick and served as the overall substrate for the MS and CPW. The recessed cavity in the middle formed half of the substrate for the SL part. When printing the recessed cavity, the slope at the edge of the two sides was naturally formed due to the overspray of the polyimide ink and the liquid status before curing. Then, layer 3 with uniform thickness was printed and formed a continuous coverage over the slope. The signal line of the SL was sandwiched by layer 2 and layer 4. Accordingly, the MS-to-SL transition

Table 8 Summary of geometries

	Design (μm)	Fabrication (μm)	Deviation (%)
d	500	500±5	1.00
s	500	500±3	0.60
h	40	38±2	5.00
t_{metal}	3.5	3±0.5	14.29
G	30	30±2	6.67
W_1	1300	1300±5	0.38
W_2	19	19±3	15.79
W_3	90	92±2	2.22
W_4	110	110±5	4.55
L_1	8000	8000±5	0.06
L_2	11400	11400±5	0.04

was embedded in the polyimide. From Section II, the minimum diameter of pre-printed holes by polyimide is 160 μm, but in order to have a good matching for the transition, the diameter has to be around 20 μm. Furthermore, to achieve a high aspect ratio, proper via metallization has to be achieved. Hence, this 3-D transition was designed here thanks to the capability of printing a non-planar surface substrate by AJP. Finally, layer 5 was deposited as the top ground, filled the printed holes previously fabricated by silver ink and connected with the bottom ground. The whole fabrication process is computer controlled via a CAD software (no masks were used).

The dimensions of the entire structure are summarized in Table 8, where d is the diameter of the vias connecting top and bottom ground planes, and s is the spacing between the vias. The parallel-plate mode, as well as the coupling of electromagnetic radiation onto digital/dc lines are suppressed with via fences connecting the two ground planes which

provides a natural shielding against incoming spurious signals in a circuit routing. A spacing of s < 5d is required to prevent a potential difference from the ground planes [77], and W_1 determines the frequency at which higher order modes will be excited. W_2, W_3, W_4 are the widths of the signal lines in SL, CPW and MS, respectively, and G is the gap between the signal line and the ground for the CPW section. Note that the selected values of d, s and h are based on the availability from manufacturing restrictions: The substrate thickness h is selected based on the maximum thickness without an internal curing step; d and s are chosen to avoid the vias merged by polyimide printing. With the aid of these values, the characteristic impedance of the SL is from (19) calculated in [79]

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_r}} \frac{h}{W_e + 0.441h} \quad , \tag{19}$$

where W_e is the effective width of the center conductor and h is the height of the substrate. Z_0 is designed as 50 Ω here. At low frequency, the conductor loss α_c is the dominant factor which can be derived in [79] as

$$\alpha_c = \frac{2.7 \times 10^{-3} R_s \varepsilon_r Z_0}{30\pi\ (h - t)} A \ \text{Np/ m} \ , \tag{20}$$

where t is the metal thickness, Rs is the RF resistance, εr is the dielectric constant of the material, and A is the coefficient defined in [79].

At high frequency, the dielectric loss α_d is prevailing, and given by

$$\alpha_d = \frac{k\ tan\delta}{2} \ \text{Np/ m} \, , \tag{21}$$

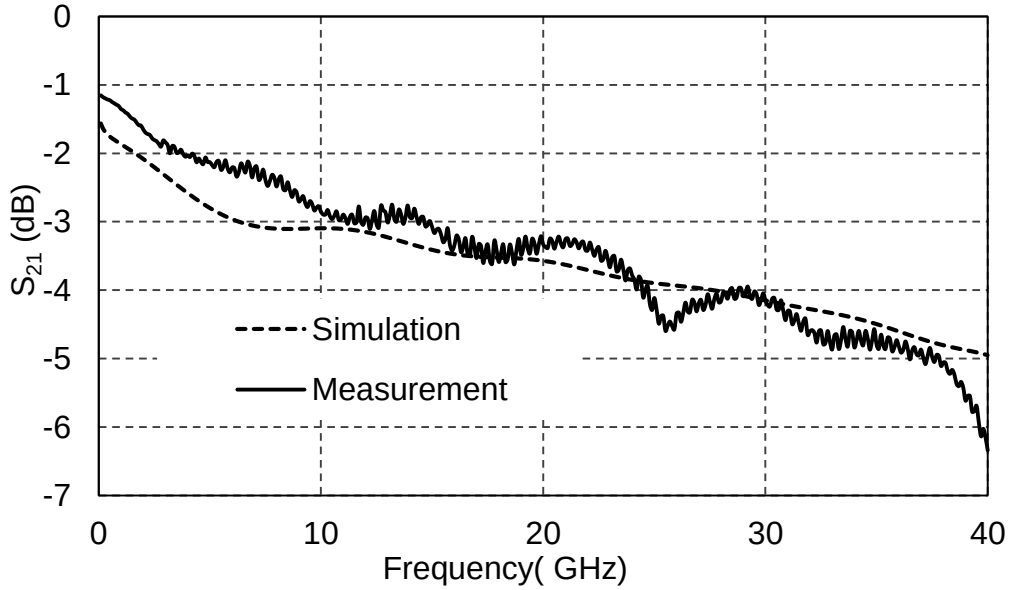
where k is the wave number and tanδ is the loss tangent of the dielectric material.

Two samples have been fabricated and their photographs are shown in Figure 36 (a). Sample 2 is used to de-embed the loss from CPW pads and transitions. The dimensions of sample 1 are summarized in Table 8 and compared with the designed values. It is shown that the planar fabrication deviation is less than 5 μm and the total alignment is within 10

μm after a 40 μm thick multilayer stacking for both silver ink and polyimide ink. The surface roughness of sample 1 is 1.5 μm and sample 2 is 4.8 μm. The fabrication error also largely depends on the size of the deposit-nozzle as well as the properties of the materials.

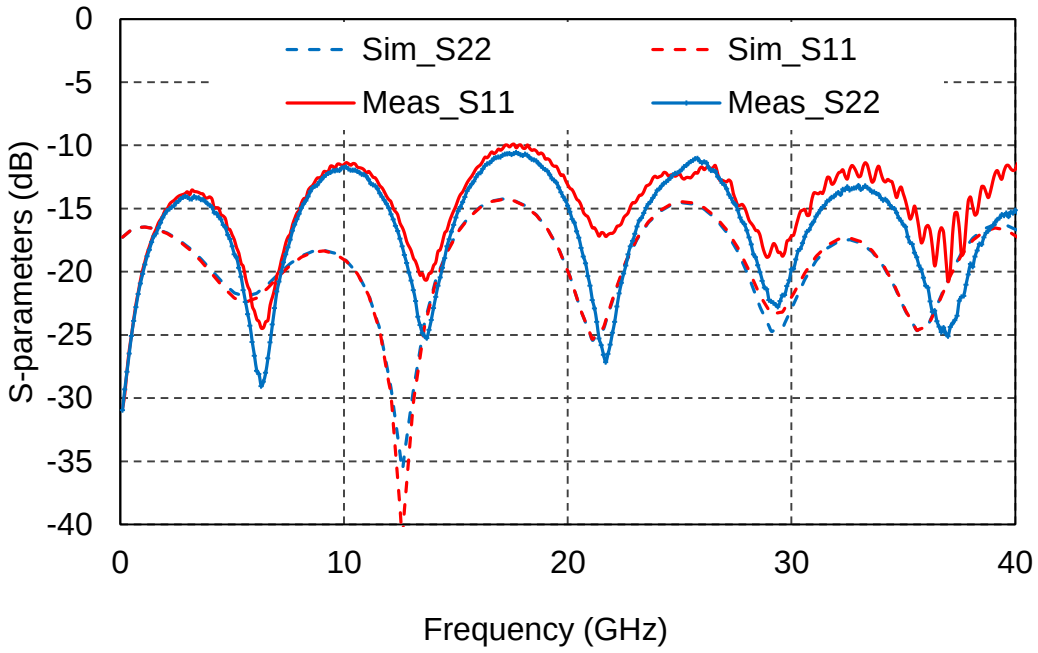
5.3.2 Measurement

An Agilent 8517B vector network analyzer is used to perform S-parameters measurements. 250 μm pitch GSG Probes are used with an SOLT calibration. The reference planes are located at the feeding CPW pads. The simulation is based on the designed dimension with 1.5 μm surface roughness in ANSYS HFSS. The measurement results agree well with the simulations for the long sample as shown in Figure 34 and the measurement results of the short sample is shown in Figure 35. Good matching is achieved below 40 GHz for both samples.



(a)

Figure 34. (a) Measured and simulated insertion loss of the sample 1 with a total length of 11.4mm. (b) Measured and simulated return loss of the sample 1 with a total length of 11.4mm.



(b)

Figure 34 continued.

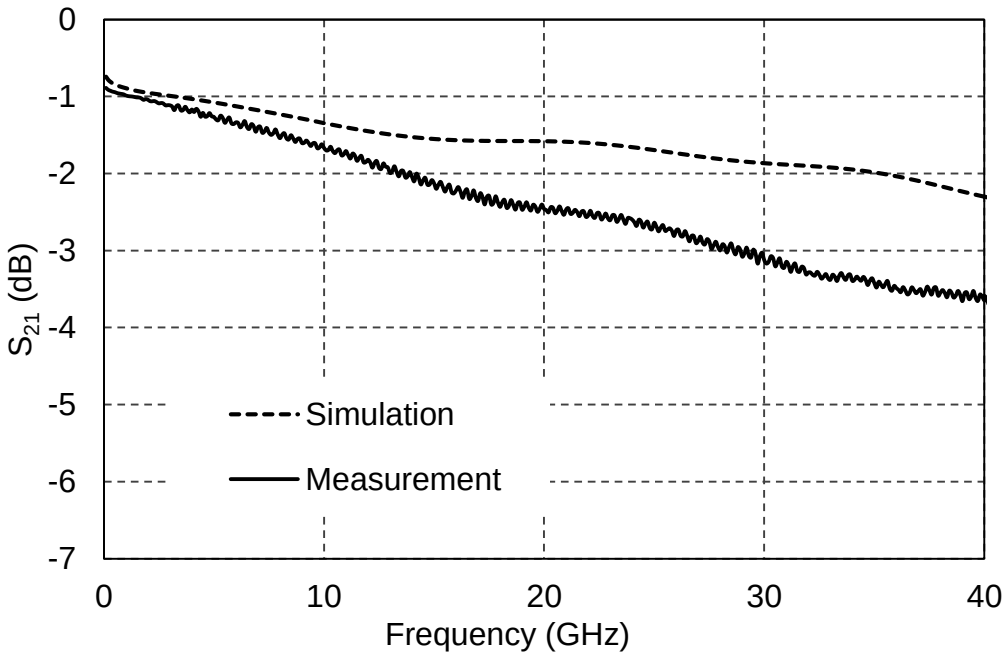
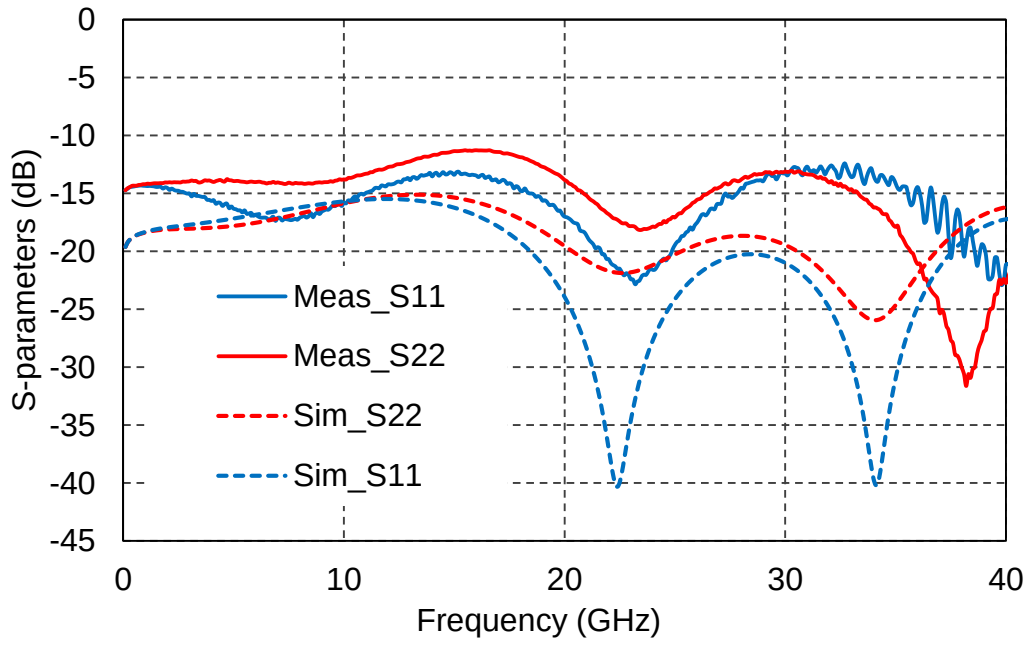


Figure 35. (a) Measured and simulated insertion loss of the sample 2 with a total length of 6.4mm. (b) Measured and simulated return loss of the sample 1 with a total length of 6.4mm.



(b)

Figure 35 continued.

Additional loss of the short one is attributed to the increased roughness. Measurements also show an insertion loss (IF) of 1.2 dB at 1 GHz and 6.3 dB at 40 GHz for the 11.4 mm sample. Compared with the longer sample, the insertion loss of the 6.4 mm sample is 0.9 dB at 1 GHz and 3.6 dB at 40 GHz. Note that this insertion loss is a combination of the losses from the stripline, CPW pads, MS lines and transitions. Considering the shorter

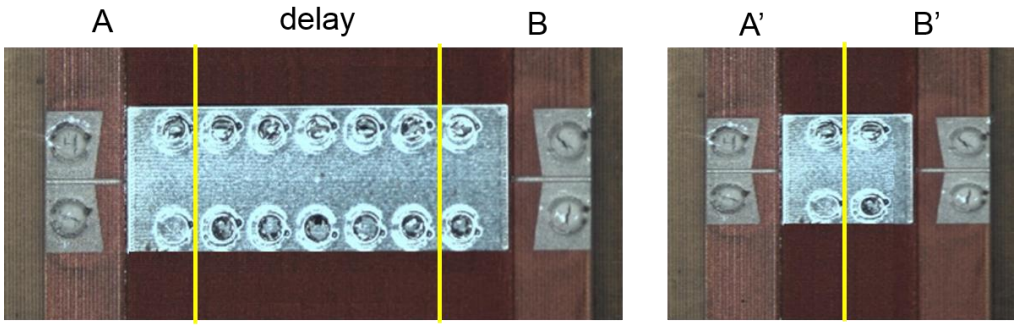
sample as a back-to-back configuration and the longer sample as the standard one with a delay line, the chain transmission matrices of the two samples can now be expressed by

$$(T_{standard}) = (T_A) \cdot \left(T_{delay}\right) \cdot (T_B) \tag{22}$$

$$(T_{back-back}) = (T_{A'}) \cdot (T_{B'}) \tag{23}$$

$$\left(T_{delay}\right) = \begin{pmatrix} e^{-\gamma L} & 0 \\ 0 & e^{-\gamma L} \end{pmatrix} \tag{24}$$

where T_A, T_B and T_{delay} represent the matrices for A, B and delay of the stripline in Figure 36 (a). Based on the very small fabrication errors (less than 5 μm) on the dimensions of the MS and CPW lines, the change in the characteristic impedance is negligible. Thus, assuming (T_A) equals ($T_{A'}$) and (T_B) equals ($T_{B'}$), the insertion loss of the SL is extracted by subtracting the S_{21} of two prototypes and the result is shown in Figure 36 (b). For the AJP fabricated stripline, the extracted line loss is 0.03 dB/mm at 1 GHz, 0.33 dB/mm at 30 GHz and 0.53 dB/mm at 40 GHz. Compared with the measured loss of 0.62 dB/mm at 30 GHz on a 17.3 μm polyimide substrate, and the calculated loss (with ADS LineCalc) of 0.2 dB/mm at 30 GHz based on a 40 μm thick polyimide in [80], the AJP fabricated stripline compares very well providing almost identical loss values.



(a)

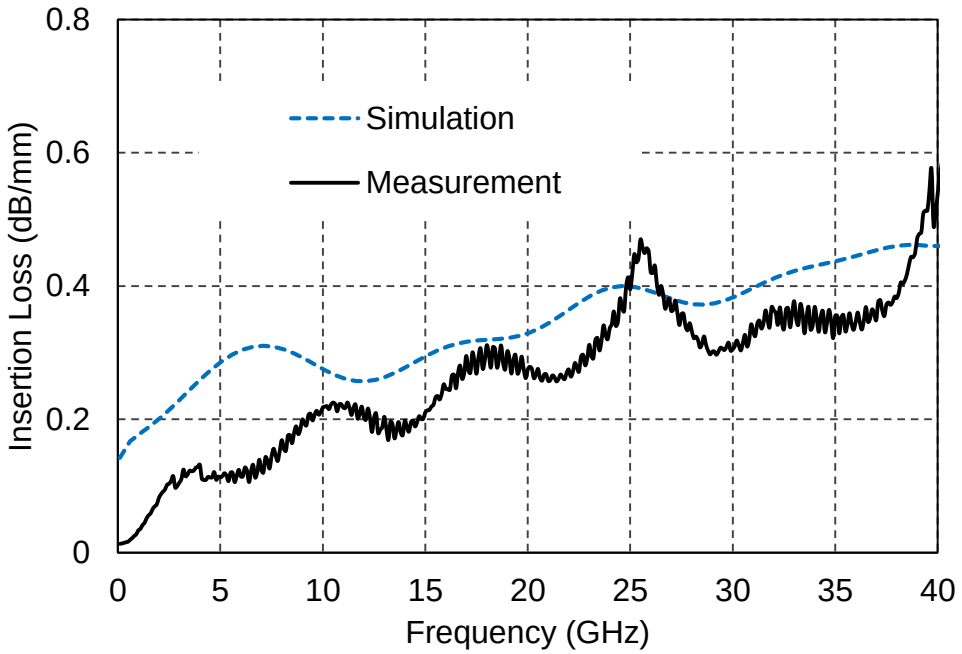


Figure 36. (a) Two samples with the de-embedded position marked in yellow. (b) Extracted insertion loss of the stripline.

5.3.3 Conclusions

Utilizing aerosol jet printing (AJP) as a digital deposition method, printed multilayer interconnects with vertical transitions are demonstrated and characterized up to 40 GHz for the first time. In the dissertation, we assess the availability of the printed materials for RF applications, investigate the process conditions of various materials, and design multiple interconnects with vertical transitions. Multilayer interconnects are

measured up to 40 GHz showing competitive RF performance. Fine-pitch size of a single line is demonstrated as small as 10 μm for silver ink and 80 μm for polyimide. The embedded via with a slope achieved a width as small as 19 μm through a 20 μm thick polyimide and the proposed fabrication process indicates the potential to achieve a higher aspect ratio in the embedded vias. The polyimide based stripline loss is extracted to be 0.33 dB/mm at 30 GHz and 0.53 dB/mm at 40 GHz. Good matching is achieved from DC to 40 GHz as the accurate fabrication enables the 30 μm gaps with an error of less than 5 μm. This work paves the way for digital printing as a promising technology for mm-wave applications, and indicates a fast and cost efficient method to design complex 3-D structures in the future.

CHAPTER 6

RF CAVITY COMPONENTS BY 3-D PRINTING TECHNOLOGY

6.1 Introduction

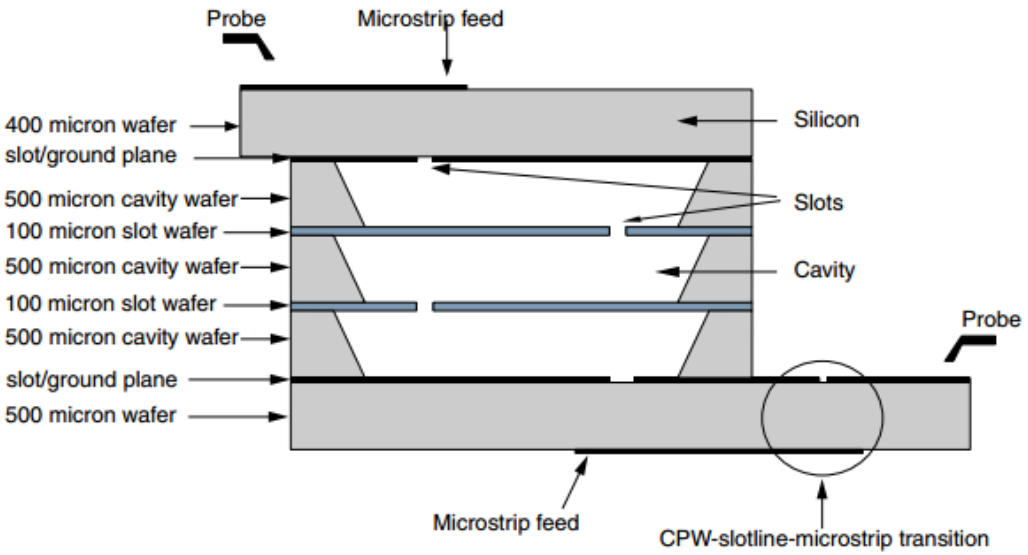
The rapid development of a low-cost, lightweight high-Q X-band resonator and bandpass filter implemented by Polyjet printing technology is presented in this chapter. The technique achieved 16 μm at individual layer thickness and the horizontal fabrication deviation was less than 0.5%. A single cavity resonator and a vertical stacked filter are analyzed and built. The theoretically calculated results are well-matched with measurements. The fabrication process has been simplified as much as possible and only takes two steps: printing resin and sputtering or electroplating copper. The final parts were measured without tuning while the surface was not subjected to any post finishing process.

In this dissertation, the cavity components are achieved by Polyjet Printing technique which is one of 3-D printing technologies. An investigation to fabricate and assembly the structure is analyzed in detail through EM field analysis. In addition, the the model of the surface roughness is built and gives a further guidance for the 3-D printed part's performance optimization.

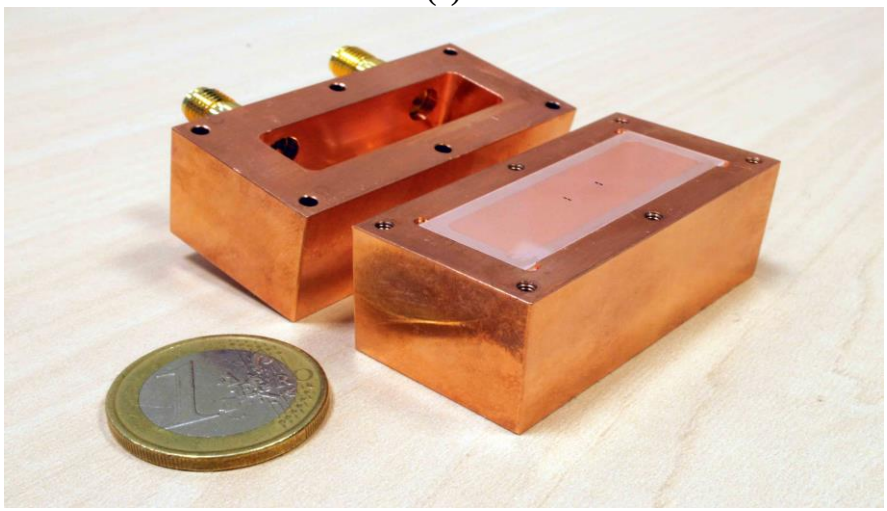
6.2 Resonator

The work presented began with the investigation of how the band-width and the response of a single X-band cavity resonator would be affected by characterizing the processing technique. The finite-element method (FEM) was used in the theoretical analysis to compute the EM fields inside the cavity with the aid of Ansys High Frequency Structure Simulator (HFSS).

Typically, there are two ways to feed a cavity resonator shown in Figure 37. The micromachined cavity is fed by two coupled microstrip lines through two slots. This structure can be used as a microwave high Q resonator for the development of narrowband loss filters in a planar environment [47]. This approach makes it difficult to make a fine pattern on the thick cavity and an embedded pattern inside the cavity. The other way is to use connectors to feed the cavity directly [48]. This approach, with its bulky body and heavy weight, is more straightforward and avoids the uncertain loss by the connectors.



(a)



(b)

Figure 37. Cavity resonator feeding approaches [47], [48].

A typical rectangular resonator is shown in Figure 38 (a). It can be represented as two resonant circuit shown in Figure 38 (b) and (c) [79].

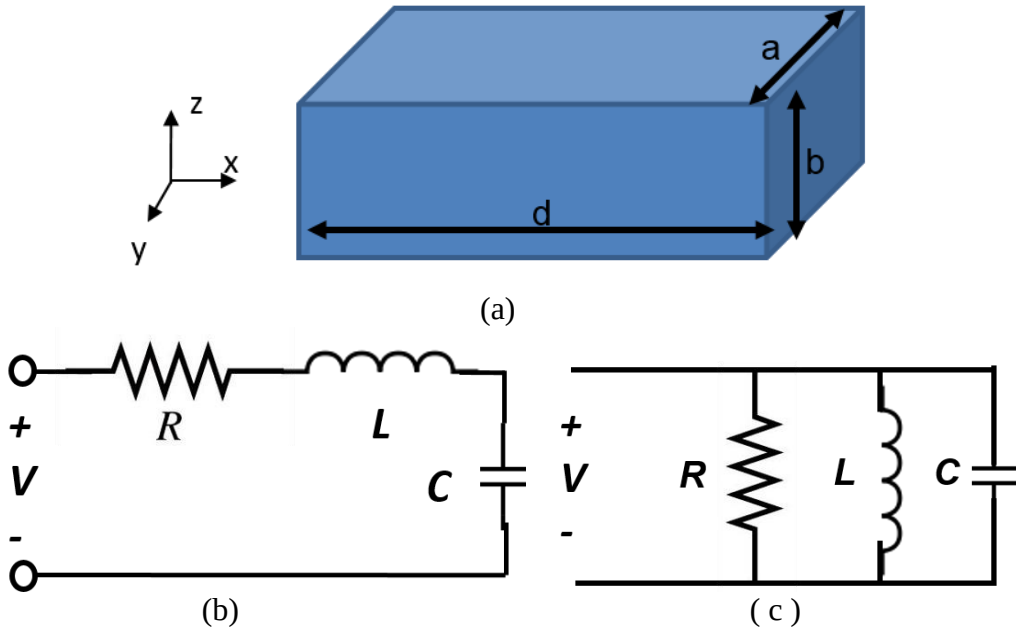


Figure 38. (a) A rectangular resonator that has the propagation direction in Z. (b) The equivalent circuit with LCR in series. (c) The equivalent circuit with LCR in parallel.

The input impedance is

$$Z_{in} = R + j\omega L - \frac{1}{\omega C} \tag{25}$$

or

$$Z_{in} = (\frac{1}{R} + \frac{1}{j\omega L} + j\omega C)^{-1} \tag{16}$$

The resonant condition in the circuit is when the inductive reactance cancels the capacitive reactance, so the resonant frequency is

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{27}$$

The average electric energy stored in the capacitor and the inductor under a sinusoidal voltage is

$$W_C = \frac{1}{4}C|V_C|^2 = \frac{1}{4}|I|^2\frac{1}{\omega^2 C} \tag{28}$$

and

$$W_L = \frac{1}{4}L|I|^2 = \frac{1}{4}|V|^2\frac{1}{\omega^2 L} \tag{29}$$

The input impedance at the resonant condition is purely resistive at the resonant frequency and the complex power delivered to the resonator is

$$P_{in} = \frac{1}{2} V I^* = \frac{1}{2} |I|^2 Z_{in} \tag{30}$$

The unloaded quality factor for the resonant circuit, is defined as the ratio of the energy stored in the resonant circuit to the power loss in the resonant circuit at the resonant frequency,

$$Q_u = \frac{\omega_0 L}{R} = \frac{L}{\omega_0 RC} \tag{31}$$

The resonant cavity as illustrated in Figure 39 is a waveguide with propagation direction z.

The rectangular waveguide mode for E transverse to z is given by

$$\bar{E}(x, y, z) = \bar{e}(x, y)[A^+ e^{-j\beta_{mn} z} + A^- e^{-j\beta_{mn} z}] \tag{32}$$

where A^+ and A^- are amplitudes for forward and reverse travelling waves, respectively, and where the e(x,y) term encompasses the transverse variations in x and y. The propagation constant β_{mn} is given by

$$\beta_{mn} = \sqrt{k^2 - \left(\frac{m\pi}{a}\right)^2 - \left(\frac{n\pi}{b}\right)^2} \tag{33}$$

where k is the wavenumber which equals $\omega\sqrt{\mu\varepsilon}$, μ and ε are the permeability and permittivity of filling material in the waveguide. For the resonator presented in this dissertation, the cavity is air so that μ and ε are μ_0 and ε_0.

The boundary condition of the cavity is $\bar{E}(x, y, z) = 0$ when z = (0,d), yielding $\beta_{mn} d = l\pi$ where l is an integer multiple of $\lambda_g/2$ at the resonant frequency. The cutoff wavenumber is given by

$$f_{101} = \frac{c}{2\pi\sqrt{\mu_r \varepsilon_r}} \sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2 + \left(\frac{l}{c}\right)^2} \tag{34}$$

where a = 20.2 mm, b = 5 mm, and d = 21.4 mm are the width, height, and length of the cavity, respectively. m = l=1, n = 0 are the indexes for the 101 mode. f_{101} was calculated to be 10.2 GHz.

Given a finite conductivity, the Q of the resonator due only to the lossy walls is given by [79]

$$Q_{cond} = \frac{(kad)^3 b\eta}{2\pi^2 R_s} \frac{1}{2l^2a^3b + 2bd^3 + l^2a^3d + ad^3} \tag{35}$$

where η is the intrinsic impedance and R_s is the conductor surface resistivity and is given by

$$R_s = \sqrt{\frac{\omega\mu_0}{2\sigma}}. \tag{36}$$

Meanwhile, the loss due to the dielectric medium is negligible for an air-filled cavity, so Q_u is simply equivalent to $Q_{cond.}$

The loaded Q_l of the cavity is defined as:

$$Q_l = \frac{f_0}{\Delta f_{3-dB}} \tag{37}$$

where f_0 = 10.26 GHz is the measured resonant frequency and $\Delta f_{3\text{-dB}}$ = 0.05 GHz is the 3 dB bandwidth shown in Figure 41. Based on (2) the loaded quality factor was measured to be 205. The weaker coupling observed in the measurement as compared to the simulation is due to the contact space between the connectors and the resonator. The external Q_{ex} of the resonator can be derived from the following equation:

$$S_{21}(dB) = 20log_{10}\frac{Q_l}{Q_{ex}} \tag{38}$$

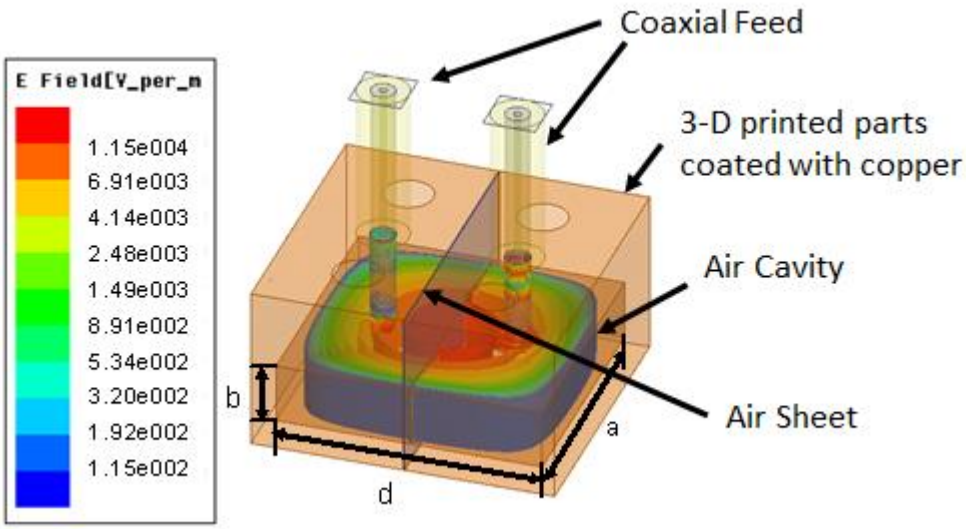


Figure 39. HFSS model of the cavity resonator with proposed assembly approach for 3-D printing fabrication.

Based on Q_{ex} and Q_l, we can calculate Q_u from Equation (4) and it is found to be 214.

$$\frac{1}{Q_l} = \frac{1}{Q_u} + \frac{1}{Q_{ex}} \tag{39}$$

The slight difference between the measured and simulated values of the unloaded quality factor can be attributed to possible increased surface roughness inside the walls of the fabricated cavities and non-idealities in the metal coverage of the resin material. This issue is still under investigation.

The proposed cavity resonator was made in two pieces by Polyjet Printing with the assembly plane in the middle of E field, as illustrated in simulation model found in Figure 39. No obvious electric field distortion or degradation was found because the assembly plane was parallel to the E-field. After generating raw 3-D parts, they were metallized by DC sputtering that can also be replaced by a low cost electroplating process. Finally, they were assembled along the vertical center plane. The fabrication process is shown in Figure 40.

The fabricated resonator was measured using K-band connectors (Pasternack connectors PE44217). The measured results are shown in Figure 41. There is very good agreement between the calculated and measured responses for the resonant frequency which is very sensitive to the dimensions. The small discrepancy in the resonant frequency can be attributed to fabrication tolerances and the surface roughness. Since the fabrication tolerance is 16 μm as characterized in Chapter II, the surface roughness effect, which will be discussed in the next section, is more pronounced.

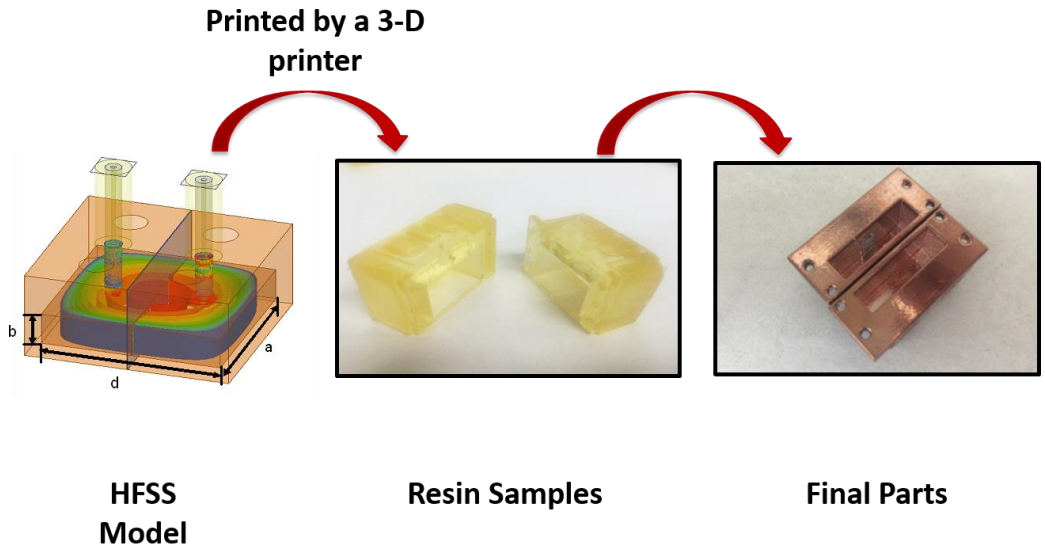


Figure 40. Fabrication process for the resonator from model to final products.

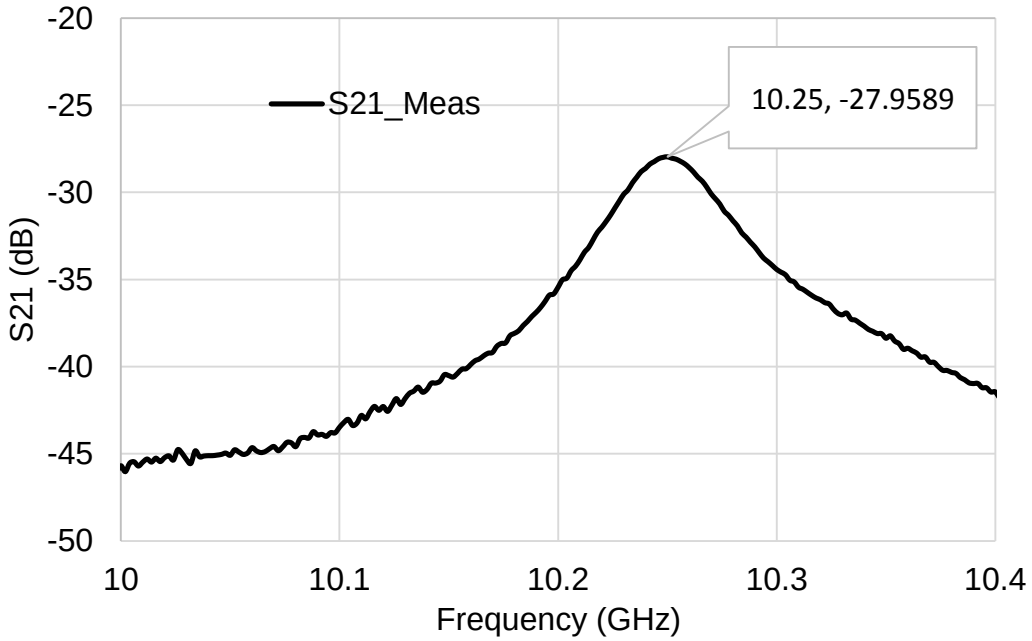


Figure 41. Measured S_{21} response.

6.3 3-D Printed Filter

An ideal filter is expected to have infinite transmission attenuation in the stopband and zero transmission attenuation in the passband while maintain a prefect linear phase response with respect to frequency, i.e., no phase distortion. Typically, a filter design flow starts from the transfer function that determins the poles, zeros as well as the input impedance.

A resonator has a reactance slope which is given by

$$\alpha = \frac{\omega_0}{2}\frac{dX}{d\omega}|_{\omega_0} \tag{40}$$

where *X* is the reactance of the resonator. First, *L*, *C* values can be given by equations from Porzar's book [79] to get a low pass filter. For a bandpass filter, with the aid of Equation 40,

$$jX_k = j\frac{\omega_1'}{\Delta}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)L_k \tag{41}$$

$$a_j = \frac{\omega_0}{2}\frac{d}{d\omega}\left[\frac{\omega_1'}{\Delta}(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega})L_k\right] \tag{42}$$

Δ is the bandpass ripple bandwidth and ω_0 is the resonance frequency, as defined by the geometric mean of ω_1 and ω_2, which are the lower and upper ripple band edge frequencies, respectively. ω_1' is the frequency of the ripple band edge of the low-pass prototype. The coupling coefficient can be derived as

$$K_{01} = \sqrt{\frac{R_A a_1 \Delta}{g_0 g_1 \omega_1'}} \tag{43}$$

$$K_{j,j+1} = \frac{\Delta}{\omega_1'}\sqrt{\frac{a_j a_{j+1}}{g_0 g_1 \omega_1'}} \tag{44}$$

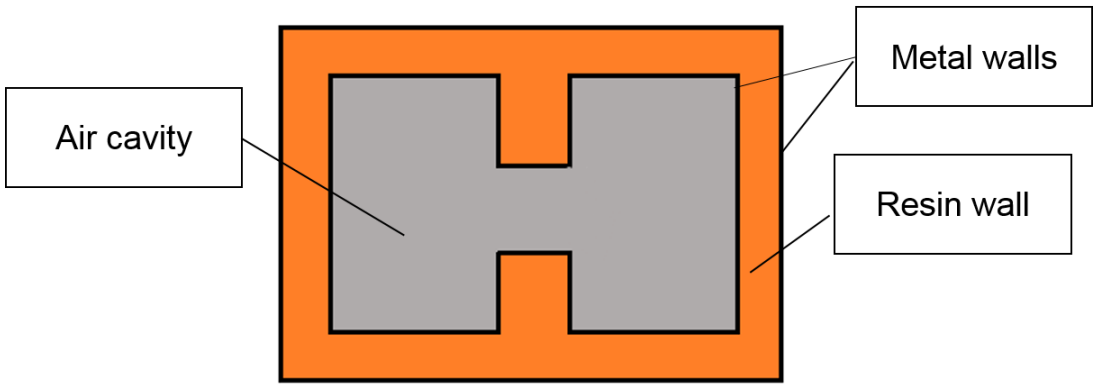
$$K_{n,n+1} = \sqrt{\frac{a_n \Delta R_B}{g_n g_{n+1} \omega_1'}} \tag{45}$$

The use of the network synthesis method and frequency transforms presented above works well for planar transmission line filters. However, for direct-coupled cavity resonator filters, only external Q and coupling coefficients between each resonator can be used to design the filter.

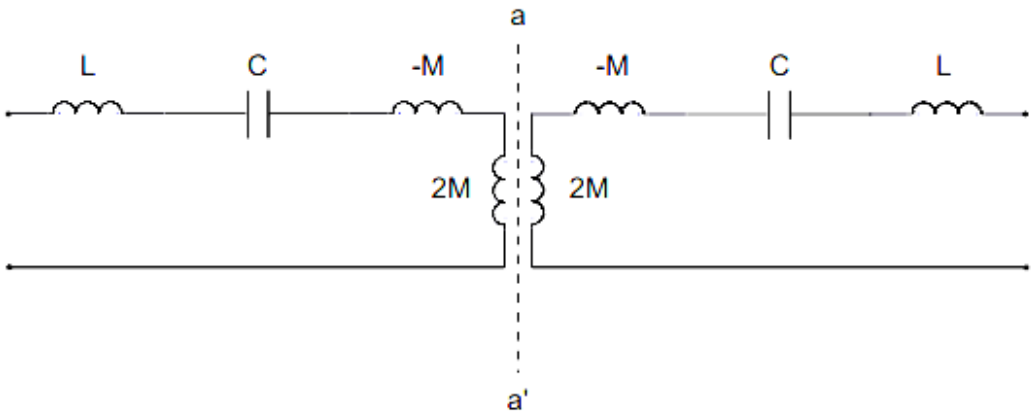
The coupling coefficients are given by

$$k_{j,j+1} = \frac{K_{j,j+1}}{\sqrt{a_j a_{j+1}}} \tag{46}$$

In Figure 42 (a), the model of a filter with two identical resonators coupled by an aperture of arbitrary thickness in their common walls is depicted. The two cavities coupled by the small aperture will exhibit the behavior of two lightly coupled identical resonant circuits, for which the equivalent circuit is shown in Figure 42 (b) [50]. The coupling slot works as a transformer and is represented as an inductance here. Equivalent inductance stands for the mutual coupling effect and presented in Figure 42 (b).



(a)



(b)

Figure 42. (a) The model of two cavities filter. (b) The equivalent circuit with the coupling reactance divided by two [79].

From this structure, the coefficient of coupling K of the equivalent circuit for the coupled cavity resonators, equals Eq. (47)

$$k = \frac{f_e^2 - f_m^2}{f_e^2 + f_m^2} \tag{47}$$

where f_e and f_m represent an electric wall and a magnetic wall at the symmetry plane respectively. They are determined by

$$f_e = \frac{1}{2\pi\sqrt{(L-M)C}} \tag{48}$$

$$f_m = \frac{1}{2\pi\sqrt{(L+M)C}} \tag{49}$$

With the preceding analysis, a Chebyshev filter with a 0.1 dB ripple, two resonators and a 3% bandwidth is chosen as to demonstrate the design flow for the 3-D printing concept. No specific insertion loss or stopband rejection goals were set for this design. From [49]

$$k_{i,i+1} = \frac{BW}{\sqrt{g_i \cdot g_{i+1}}} \tag{50}$$

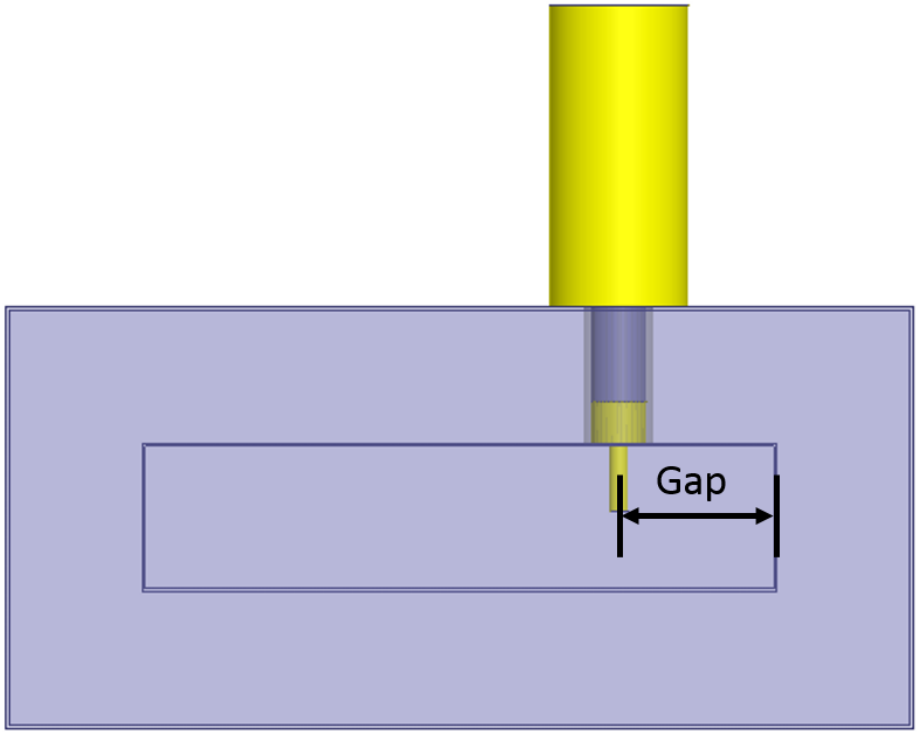
$$Q_{ex1} = \frac{g_0 \cdot g_1}{BW} \tag{51}$$

$$Q_{exN} = \frac{g_N \cdot g_{N+1}}{BW} \tag{52}$$

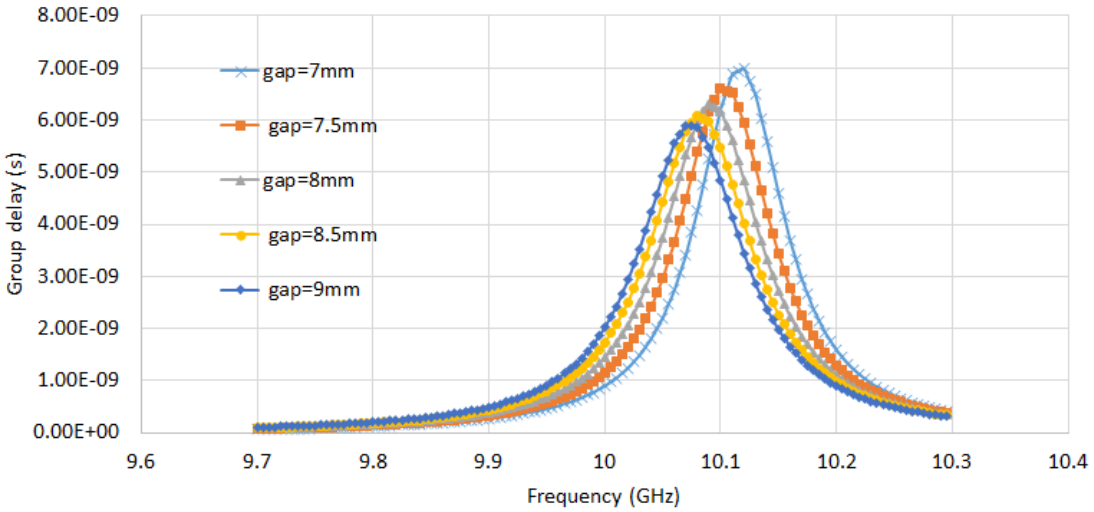
where BW is the fractional bandwidth of the filter equal ripple.

From the Chebyshev lowpass prototype table in [49] and Eq. (50)-(52) , it is found that $K_{1,2}$ = 0.01 and the required Q_{ex} is 81.

$$Q_{ex} = \frac{\pi f_0 t_d}{2} \tag{2}$$



(a)



(b)

Figure 43. (a) HFSS model of the simulation for group delays. (b) Group delays versus gap.

First, the group delay versus the position of the feeding connector in a single cavity resonator is swept in HFSS as shown in Figure 43 (b) and it is found that t_d is required to be 5.1 ns to meet the desired *Q*ex. Then two identical resonators are weakly coupled and the coupling coefficient is shown in Figure 44. The overhang structure is oriented vertically, therefore, it cannot be monolithically fabricated using traditional techniques such as micromachining and conventional printing. After the optimization based on the above sweep to get the input impedance matching and proper coupling coefficient, the configuration of the filter is described as in Figure 45. Each resonator has dimensions of 20.2 mm × 21.4 mm × 5 mm. The iris aperture is 6.2 mm wide. The wall of the resin is designed to be 3.18 mm thick for properly securing the excitation probes at the feeding position. The geometry of the two cavity filter is described in Figure 45 .

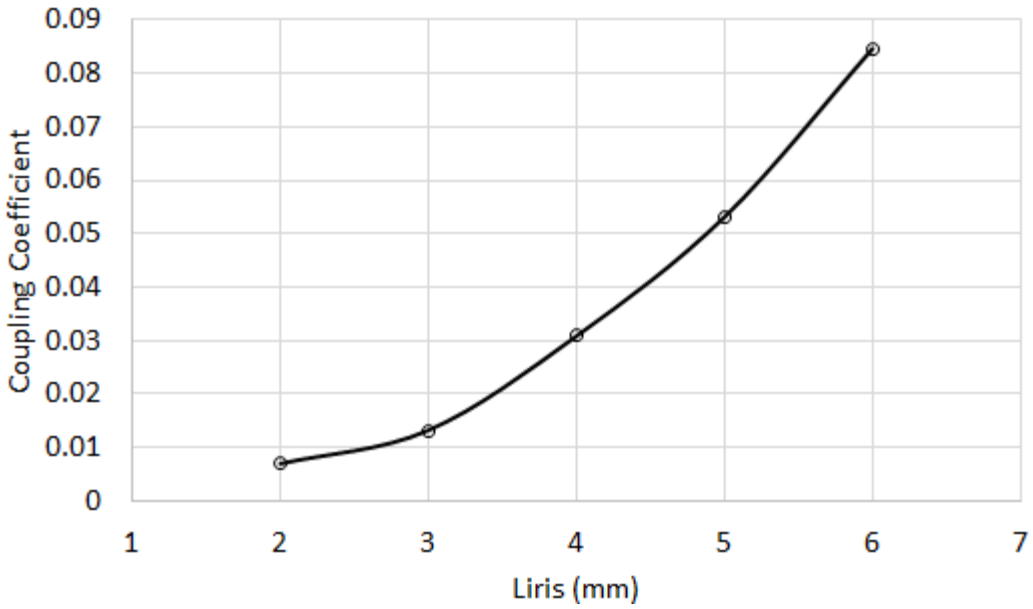
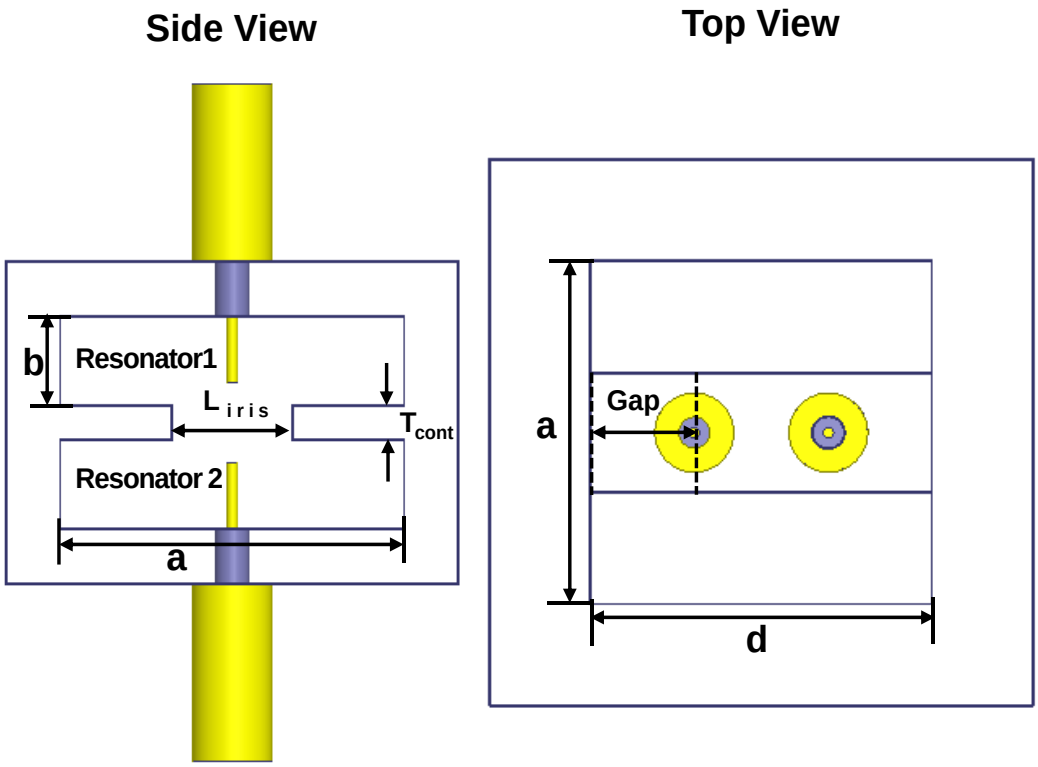
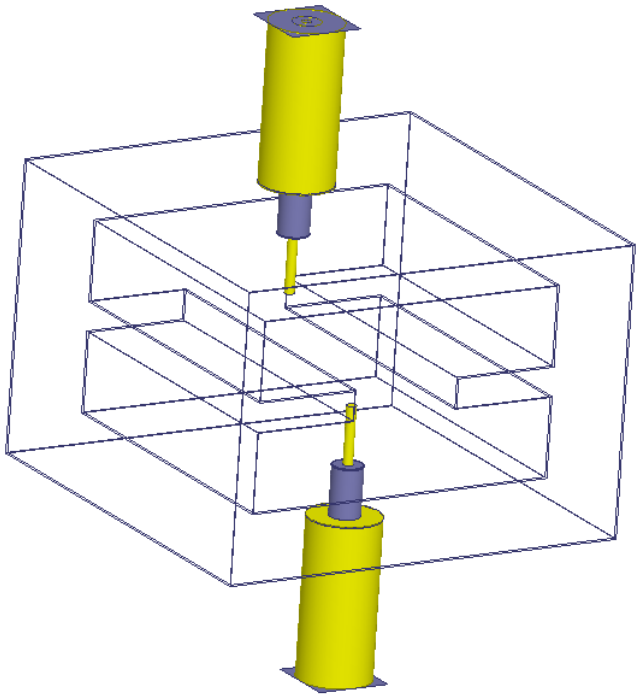


Figure 44. Coupling coefficient k versus the coupling slot width Liris, curve fit to HFSS simulation results.



(a)



(b)

Figure 45. (a) The top view and side view of vertical integrated filter. (b) 3-D view of the filter with vertical coupled resonator.

Table 9 Fabrication tolerances & resonator's frequency

	Des. (mm)	Fab. (mm)	Deviation
a	20.20	20.18	0.1%
b	5.00	4.98	0.4%
d	21.4	21.21	0.42%
L_{iris}	6.20	6.19	0.16%
T_{cont}	1.85	1.85	0.11%
Gap	6.00	6.01	0.17%
f_c	20.2	20.26	0.3%

The resonator and the filter were fabricated by the Objet Eden 250 system shown in Figure 14 (in Chapter II) with UV curable resin. Aside from the fact that the resolution improves to a large extent, the fabrication process is much easier than traditional photolithography. The fabrication process only includes two steps: printing the parts by the Objet Eden 250 system and sputtering 5 μm thick copper on the surface of the parts. The latter step can also be replaced by appropriate electroplating.

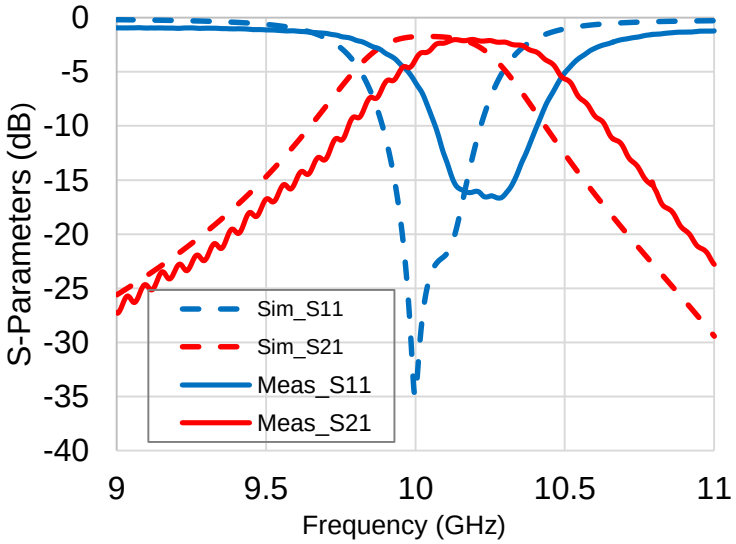


Figure 46. Simulated and measured results of the filter.

The filter was assembled with screws and the critical external coupling was achieved by using a coaxial line feed. The screws were placed inside holes that were "produced" as part of the prototype during the fabrication (no extra steps were needed for this). An SOLT calibration was performed. The reference planes for the measurement were at the edge of connectors. The measured and simulated results of the fabricated the two-pole filter can be seen in Figure 46. The small difference in the resonant frequency is due to the fabrication tolerances as well as roughness.

6.4 Surface Roughness Effect on 3-D Cavity Components

The loss arises from several different sources such as the conductive loss from the conductivity, skin depth, the dielectric loss from the tangent loss in the cavity materials, the assembly way and so on. The copper is a good conductor with a skin depth of 0.652 μm at 10 GHz. The loss tangent is close to zero for the air filled cavity. For the assembly, along the middle of E plane, there is no current distortion and negligible loss as shown in Figure 47. So the surface roughness is the main source of the loss. This section gives an analysis for the surface roughness analysis.

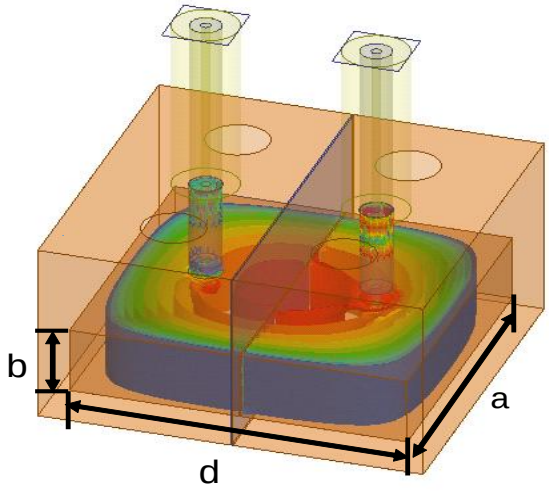
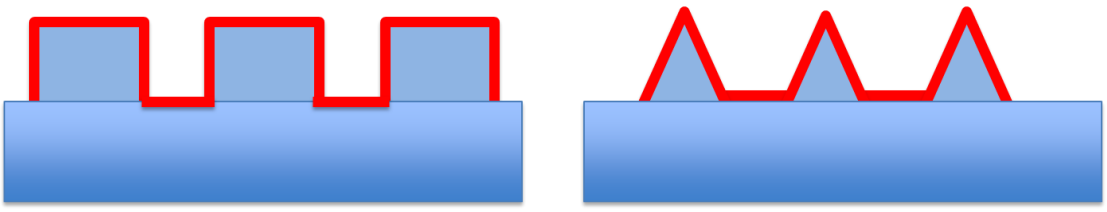


Figure 47. The E-field for a cavity resonator with a gap in the middle.

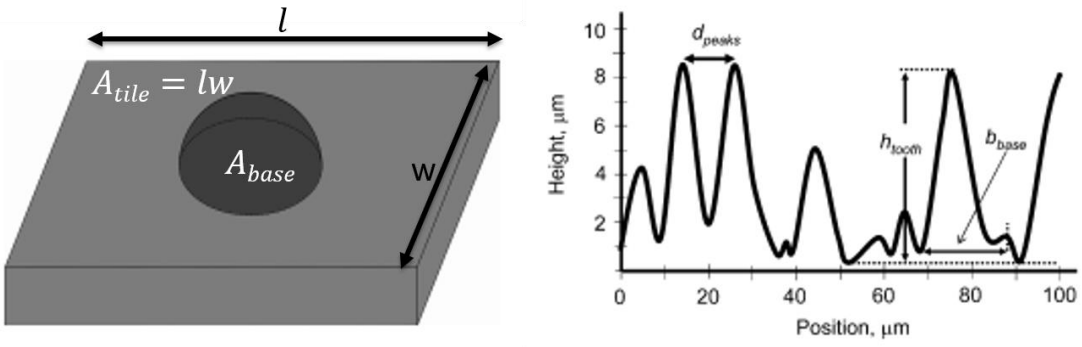
At high frequencies, currents following small imperfections on conductor surfaces increase loss. There are miscellaneous methods are proposed to account for the surface roughness effect. Luki's proposes a full-wave simulation from CAD [52]. Yet, it is independent on the frequency and, thus, inaccurate for broadband investigations in the future. Basically, there are three mathematical models used to approximate loss increase due to surface roughness: Morgan, Hammerstad and Hemispherical model.

The Morgan model, as proposed in 1949, is based on a periodic structure assumption and analyzes hypothetical transverse and parallel grooves. The study was simplified by choosing imagined rectangular and triangular grooves, namely, it assumes that current flows along the axis of periodicity as shown in Figure 48. (a) Rectangular and (b) triangular surface grooves model in Morgan Model.Figure 48. However, later engineers incorrectly interpreted his model as if the additional power absorption caused by longer current travel path length due to the surface roughness. Morgan analyzed electric field intensity in grooves parallel to the direction of propagation and concluded the power dissipation attributed to them was 36% of the impact attributed by transverse grooves. But



(a) (b)

Figure 48. (a) Rectangular and (b) triangular surface grooves model in Morgan Model.



(a) (b)

Figure 49. Simplified hemispherical shape approximating a single surface protrusion.[54]

Morgan's work is too mathematical and not practical for a simple fast analysis. Later on, Erik Hammerstad presented anempirical fit to Morgan's model as

$$k_s = \frac{P_{rough}}{P_{\ smooth}} = 1 + \frac{2}{\pi}\arctan\left[1.4\,(\frac{\Delta}{\delta})^2\right] \tag{58}$$

where *K*s is the ratio of power loss caused by a rough conductor versus a perfectly flat conductor, Δ is the RMS surface roughness and δ is the skin depth. However, this simplification has no scientific basis but just based on a guess. This metrology only roughly agrees with Morgan's results when the increased path length is less than 2.00. For 3-D printed parts, however, the surface roughness can impact the power loss much greater than a factor of 2.00. This empirical fit was useful below 4 GHz.

Afterwards, a hemispherical model was proposed by Stephen Hall [51], basing on a frequency-dependent dielectric model that calculates the loss as a combination of the power scattered and absorbed from a sphere divided by the incident flux. As shown in **Figure 49**, the total loss can be calculated [54]

$$P_{tot} = \left|-Re\left[\frac{1}{4}\eta|H_0|^2\frac{3\pi}{2k^2}(\alpha(1)+\beta(1))\right]\right| + \frac{\mu_0\omega\delta}{4}|H_0|^2\,(A_{tile}-A_{base}) \tag{59}$$

where A_{tile} is the tile area of the plane surrounding the protrusion and A base is the base area of the hemisphere. H_0 is the magnetic field on the tile and assumes it is not affected by the presence of the hemisphere. The scattering coefficients α (1) and β (1) are given as follows [54]:

$$\alpha(1) = -\frac{2j}{3}(kr)^3\left[\frac{1-\frac{\delta}{r}(1+j)}{1+\frac{\delta}{2r}(1+j)}\right] \tag{60}$$

$$\beta(1) = -\frac{2j}{3}(kr)^3\left[\frac{1-\frac{4j}{k^2r\delta}(\frac{1}{1-j})}{1+\frac{2j}{k^2r\delta}(\frac{1}{1-j})}\right] \tag{61}$$

the power of a hemisphere in Figure 49 is given by

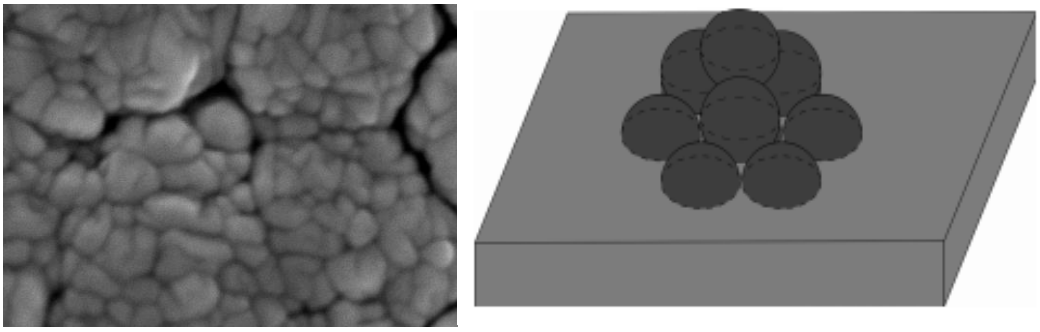
$$P_{hemisphere} = \left|-Re\left[\frac{1}{4}\eta|H_0|^2\frac{3\pi}{2k^2}(\alpha(1)+\beta(1))\right]\right| \tag{62}$$

where $\eta = \sqrt{\mu_0/\varepsilon_0\varepsilon'}$

Based on the above analysis, the ratio of the power absorbed with and without a good conducting protrusion present can be simplified as

$$k_s = \frac{\left|Re\left[\eta\frac{3\pi}{2k^2}(\alpha(1)+\beta(1))\right]\right| + \frac{\mu_0\omega\delta}{4}\,(A_{tile}-A_{base})}{\frac{\mu_0\omega\delta}{4}\,A_{tile}} \tag{63}$$

In this model, the radius of volume equivalent hemispheres are determined to computer the scattering coefficients from Eq. (61) and (62). The rms distance between



(a) (b)

Figure 50. (a) A SEM image from the surface roughness of a 3-D printed parts with copper. (b) The snowball model proposed by Paul Huray.

peaks in the roughness profile is used to calculate the tile area $A_{tile.}$ The related parameters are shown in

$$r_e = \sqrt[3]{h_{tooth}\,(\frac{b_{base}}{2})^2} \tag{64}$$

h_{tooth} is tooth height, b_{base} is tooth base width and r_e is radius of a hemisphere with equivalent volume of the tooth.

$$A_{base} = \pi(\frac{b_{base}}{2})^2 \tag{65}$$

$$A_{tile} = d_{peaks}^2 \tag{66}$$

However, this still has limits in terms of taking into account the additional scattered loss from semi-hemisphere as there several levels of spheres and more space in an actual case as shown in Figure 50 (a) for a surface image of copper foil. To fully describe the impact of the surface roughness, Dr. Paul Huray applied a first principles analysis to describe the power loss. It relies on a snowball model as in Figure 55 (b) [56].

The power loss of a conductor's rough surface with respect to a flat surface

$$k_s = \left[\frac{\mu_0 \omega \delta}{4} |H_0|^2 \, A_{Matte} + \sum_{i=1}^{j} N_i \sigma_{total,i} \frac{\eta}{2} |H_0|^2\right] / [\frac{\mu_0 \omega \delta}{4} |H_0|^2 \, A_{Flat}] \quad (67)$$

where H_0 is the local magnetic field intensity maximum in amperes/m, A_{mate} is the untreated copper foil source area without anchor nodules, A_{Flat} is the perfectly flat two-dimensional area in m^2, μ_0 is the permeability of free space in H/m, Ni is the total number of surface spherical features of radial size α_i, $\sigma_{total,i}$ is the total absorption and scattering cross sections of radial size α_i spheres in m^2, and η is the intrinsic impedance of the propagating medium in Ω. Approximating the snowballs to spheres and substituent the cross section of a distribution of j snowballs into (67) permits *k*s to be simplified as

$$k_s = \frac{A_{Matte}}{A_{flat}} + 6 \sum_{i=1}^{j} \frac{N_i \pi a_i^2}{A_{flat}} / \; (1 + \frac{\sigma}{\alpha_i} + \frac{\sigma^2}{2{\alpha_i}^2}) \quad (68)$$

where α_i is the radius of the i^{th} snowball. A_{matte}/A_{flat} is the relative surface area without snowballs per unit flat area, and Ni/ A_{flat} is the number of snowballs with radius α_i per unit flat area. The equation is embedded in Ansys HFSS software and thus can be combined

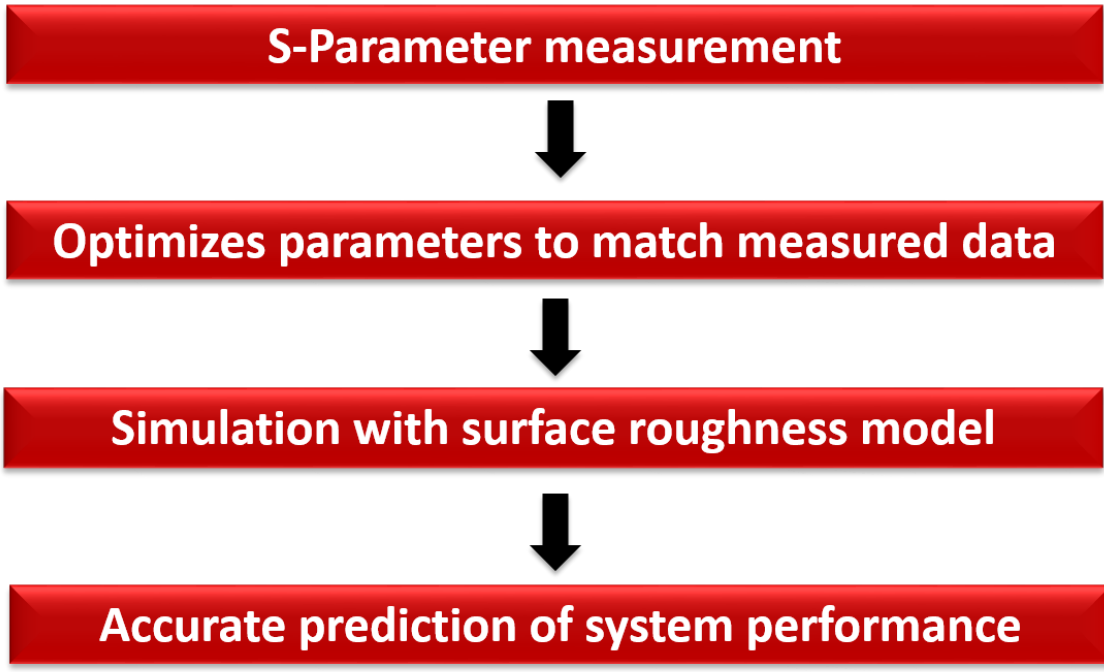


Figure 51. Design flow to extract parameters in Huray model.

into a full-wave simulation. However, it is not practical to acquire details of each particle. So these 3 parameters were fit by an estimation from VNA measurements in industry and subsequently incorporated into commercial electromagnetic field simulators. The design rules are shown in Figure 51. First the Huray model parameters are extracted from the measured resonator's performance. The simulated and measured results are shown in

Figure **52** with the same quality factor. The frequency shift was due to the dimension difference between the design and fabrication. With an optimization in HFSS, the extracted parameters are listed in Table 10. Using the same parameters, simulated results for the filter are compared with the measured results in Figure 52 . For the filter, the measured results matched closely with the simulations without any post-tuning. The measured fractional

bandwidth was found to be 5.1%, compared to 3.9% of the designed value. The measured insertion loss (IL) was 2.1 dB, matching well the simulated value of 2.0 dB. The shift of the center frequency between the simulation model and the fabricated prototype is 0.2 GHz, representing 2% variation. In addition, the return loss (RL) is better than 15 dB through the pass band.

Table 10 Extracted parameters for the Huray Model

Flat area	A_{flat}	100 µm
Number of particles	N_{i}	16
Skin depth	δ	0.652 µm
Radius of particles	a_i	1.66 µm

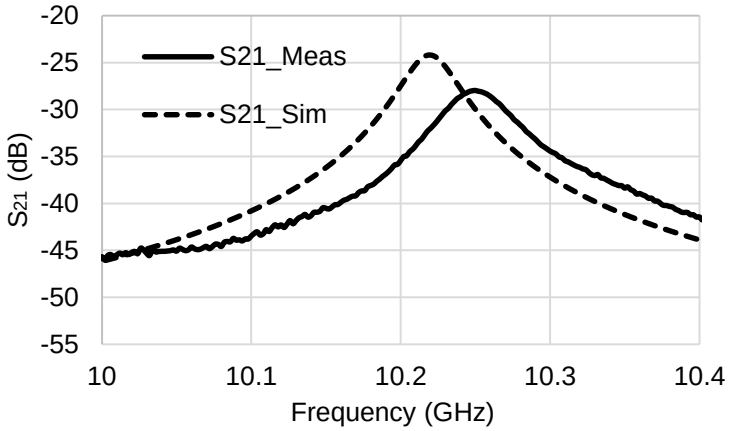


Figure 52. Simulated and measured S_{21} of the single cavity resonator.

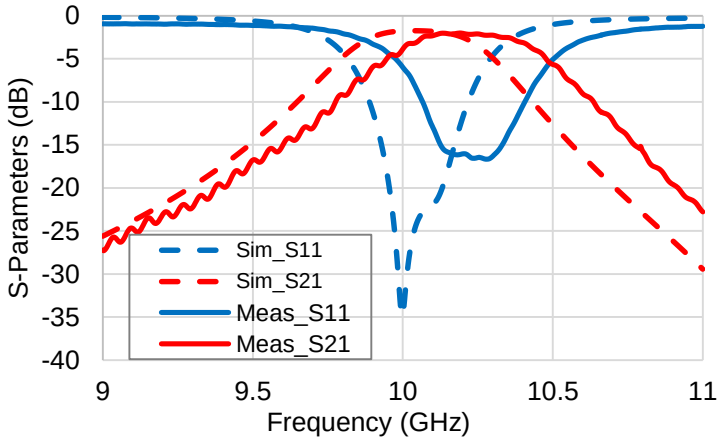


Figure 53. Simulated and measured results of the filter.

CHAPTER 7

A BROADBAND RECEIVER WITH HETEROGENOUS INTEGRATION BY 3-D PRINTING

7.1 Introduction

With the preceding analysis, the 3-D printing technology has been mature for RF/mm-wave applications. Various individual designs by 3-D printing technologies have shown a competitive performance with the ones by conventional fabrication methods regarding the fabrication time and cost and overwhelmingly RF performance compared with other additive manufacturing technologies. However, there is still very limited demonstration for broadband RF applications based on the multi-layer or 3-D system-on-package (3-D SoP) technology allowing for multiple active semiconductor components along with low-loss off-chip passives to achieve both high performance and small form factor.

This work, for the first time, demonstrates a tailorable substrate by 3-D printing and implements a broadband superhetrodyne receiver based on tailorable substrate. Our method is to use Polyjet Printing technology, which is a branch of emerging additive manufacturing technologies, to tailor the substrate with designed cavities setting thin film dies. This methods results in reduced parasitic effect and loss from the package, thus not affecting the die's original performance without the compromise of additional design steps. It shows the flexibility of exploiting a new interconnect methodology integrating heterogeneous semiconductor technologies.

7.2 A Wideband Receiver Design

For a demonstration vehicle, this prototype employs a superheterodyne receiver as shown in Figure 54, consisting of a commercially available LNA and mixer. In a practical application, it also includes passive filters to achieve band selection and image rejection which are not implemented here. Utilizing the advantage of the accuracy in Polyjet Printing technology, the cavity closely fits the die with a gap of less than 2 mil to get the wirebonding as short as possible, and, thus, mitigate effectively the parasitic effect. The wideband LNA is an Avago Technologies AMMC-6220 die fabricated by the PHEMT process to provide exceptional noise and gain performance. It operates from 6 GHz to 20 GHz with a DC bias current of 53 mA. Several 100 pF chip capacitors are used as decoupling capacitors for the supply of the LNA. The mixer (Hittite HMC 143) is a GaAs double-balanced GaAs die, made with 1 μm MESFET process. The IF bandwidth is from DC to 3 GHz. The total circuit is based on resin. Figure 54 depicts a 3-D view of the receiver package module. Given the RF properties and thickness of the resin, 50 Ω CPW to Microstrip lines were designed using Ansys HFSS. As such, the gap was 500 μm, the width of the signal line of the CPW lines was 1.01 mm, and the the width of the microstrip line was 1.10 mm.

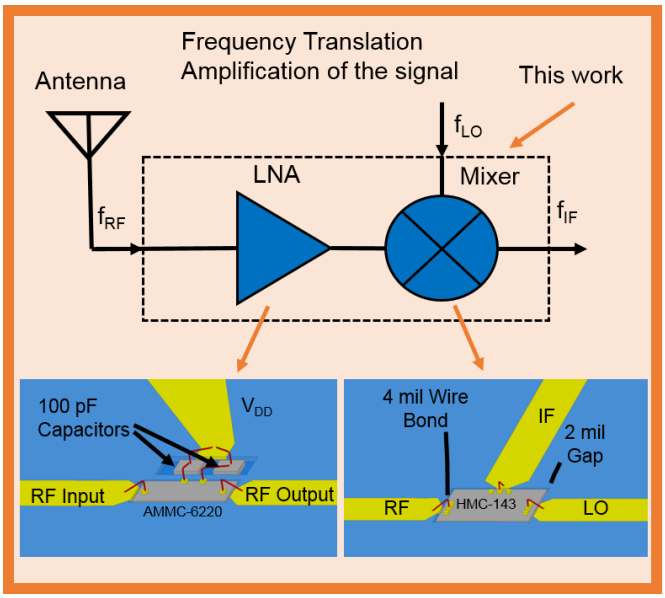


Figure 54. The receiver architecture and the related package models.

The module substrate was first produced using the Polyjet Printing Process. Using the minimum single layer thickness of approximately 20 μm, the 400 μm thick substrate was used for 50 Ω lines and three cavities were formed to attach the LNA and the mixer dies as well as the decoupling chip capacitors. Then, 50 Ω transmission lines and DC supply lines are metalized on the tailored substrate by DC sputtering. The module for the packaged die was adjusted to account for the overspray. The tailored substrates are shown in Figure 55, and a photograph of the assembled receiver module is shown in Figure 56. It takes 2 mins/ module substrate.

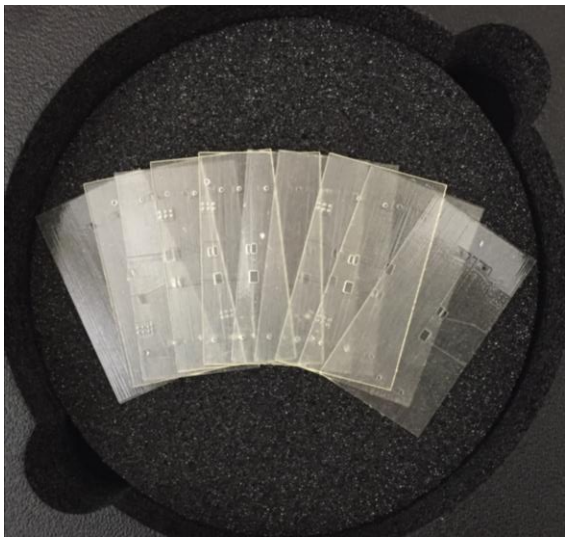


Figure 55. Tailored substrate for the receiver front-end module.

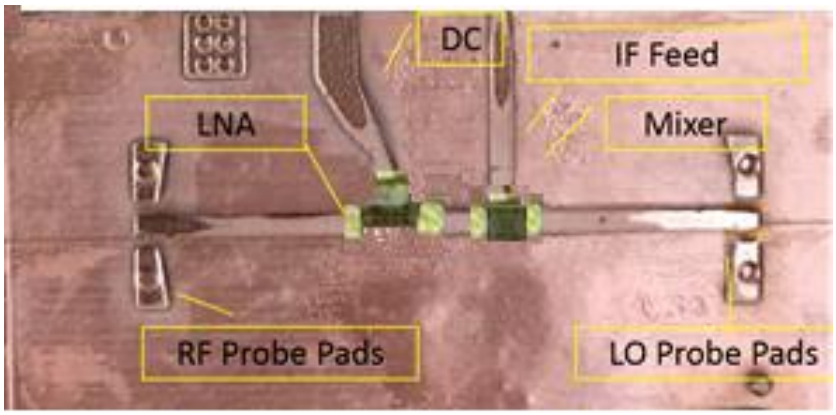


Figure 56. The receiver module sample after attaching dies.

A NIST SplitC Software was used to first estimate the dielectric properties of the resin samples. Relevant information was derived from the resonant frequency of a high-Q cylindrical resonator, which is related to the dielectric constant, and the corresponding Q-factor, which corresponds to the loss. The measured values were analyzed with the SplitC software to provide the dielectric properties. A High Frequency Structural Simulator (HFSS) simulation of the cavity was then performed to verify these characterization properties. These EM-simulated results were compared with the measurements. This iterative analysis provides the data for the material. Figure 57 shows the EM-simulated and measured results, and the resonance indicates the related dielectric constant. The extracted dielectric constant (ε_r) is 2.9 and the loss tangent ($\tan\delta$) is 0.006 at 25 GHz. Based on this characterization, 50 Ω transmission lines were designed for the package.

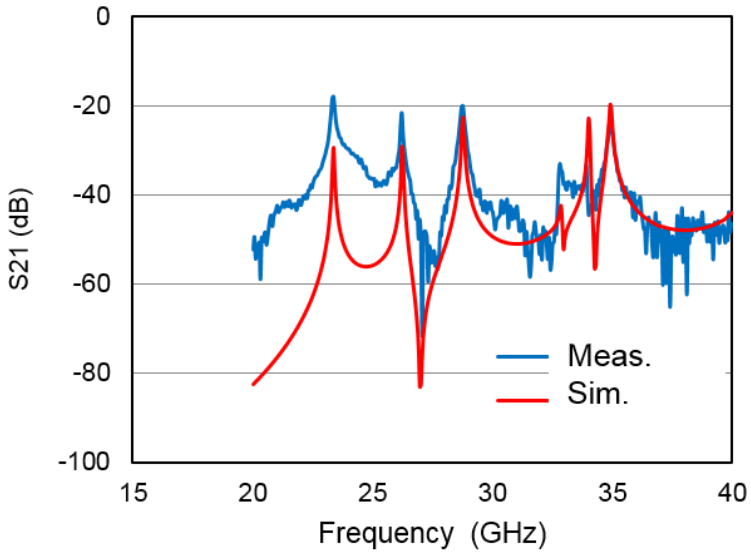


Figure 57. Characterization of the resin.

For the superheterodyne receiver measurement, a pair of ECP40-GSG-1800-DP probes from Picoprobe® were used to land at the RF and LO ports of the receiver, and an SMA connector was soldered at the IF port. The return loss at the RF port of the assembled receiver module was measured using a VNA (HP8510C). The input 50 Ω traces

and the bonding wires are simulated in HFSS. Figure 58 shows the EM-simulated and measured return loss at the RF port.

To characterize the nonlinearity of the receiver module, the input-referred 1dB compression point (P_{in1dB}) was also measured. The RF input is fed from a signal generator (HP 8360L), and the LO input is generated from another signal generator (HP 63623 B) followed by a 6-18 GHz PA (Microwave Inc.). The IF output is monitored by a spectrum analyzer (Keysight PXA N9090 A). The LO power is set as 15 dBm, and the IF frequency is set as 1.5 GHz in the linearity measurement. The RF input power of the receiver was swept from -40 dBm to 0 dBm to extrapolate the P_{in1dB}. Figure 58 shows the simulated and measured P_{in1dB} versus the RF frequency f_{RF}. Close agreement between the simulation and measurement results verifies that the extra RF routing and the bonding wires on the package has little effect of the receiver linearity. This is enabled by the precision control of the Polyjet Printing technology that forms small cavities to reduce the wire-bonding inductance.

RF-IF isolation and LO-IF isolation of the receiver module was also assessed through measurement. The RF-IF isolation in the mixer alone ranges from 30 dB to 40 dB, and the LO-IF isolation is around 20 dB.

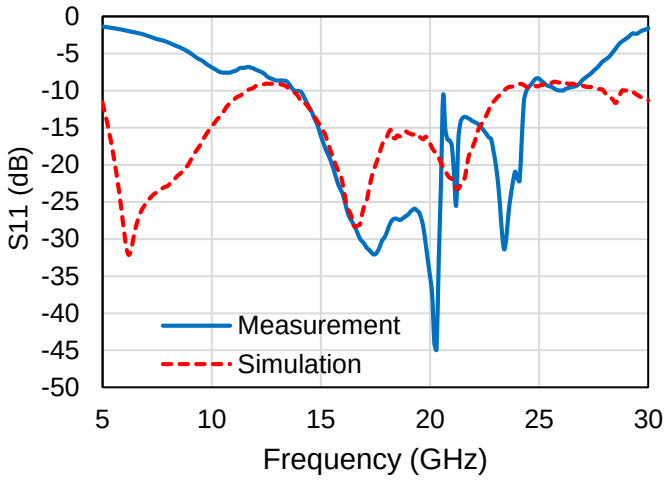


Figure 58. EM-simulated and measured return loss of the RF port in the assembled receiver module.

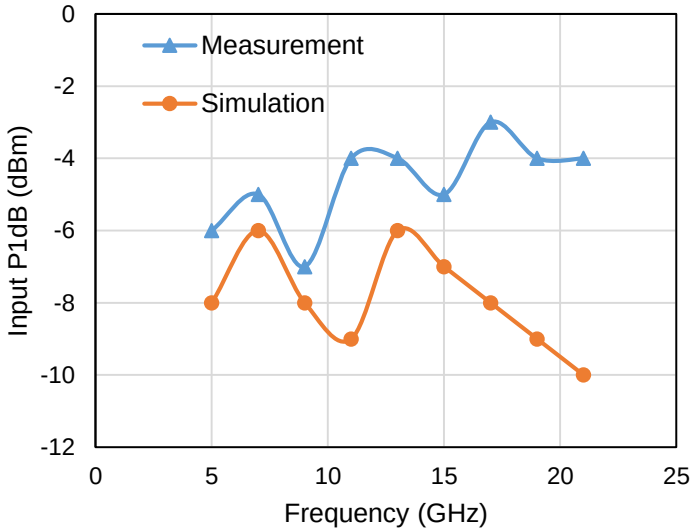


Figure 59. Input 1dB compression point of the receiver module.

In this chapter, a broadband superheterodyne receiver module was successfully assembled through Polyjet Printing technology for the first time. The contribution of this paper resides in the tailored substrate combining multilayer stacking as well as cavity etching into one step. These results pave the way for the implementation of printable and tailorable substrate as an RF substrate and package for high frequency modules and systems.

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VITA

Fan Cai was born in Hubei, China. She received the B.S. degree in electronics in Fall 2004 from Huazhong University of Science and Technology, the Master of Science and Doctor of Philosophy degree in the school of electrical and computer engineering in Fall 2011 and Spring 2016, respectively, from the Georgia Institute of Technology, Atlanta, GA. From 2009 to 2015, she worked in the Microwave Circuit Technology Group, Georgia Institute of Technology. Her doctoral research focused on 3-D printed front-end technologies, filter designs, cavity waveguide designs and applications of RF components on wearable devices and smart grids.